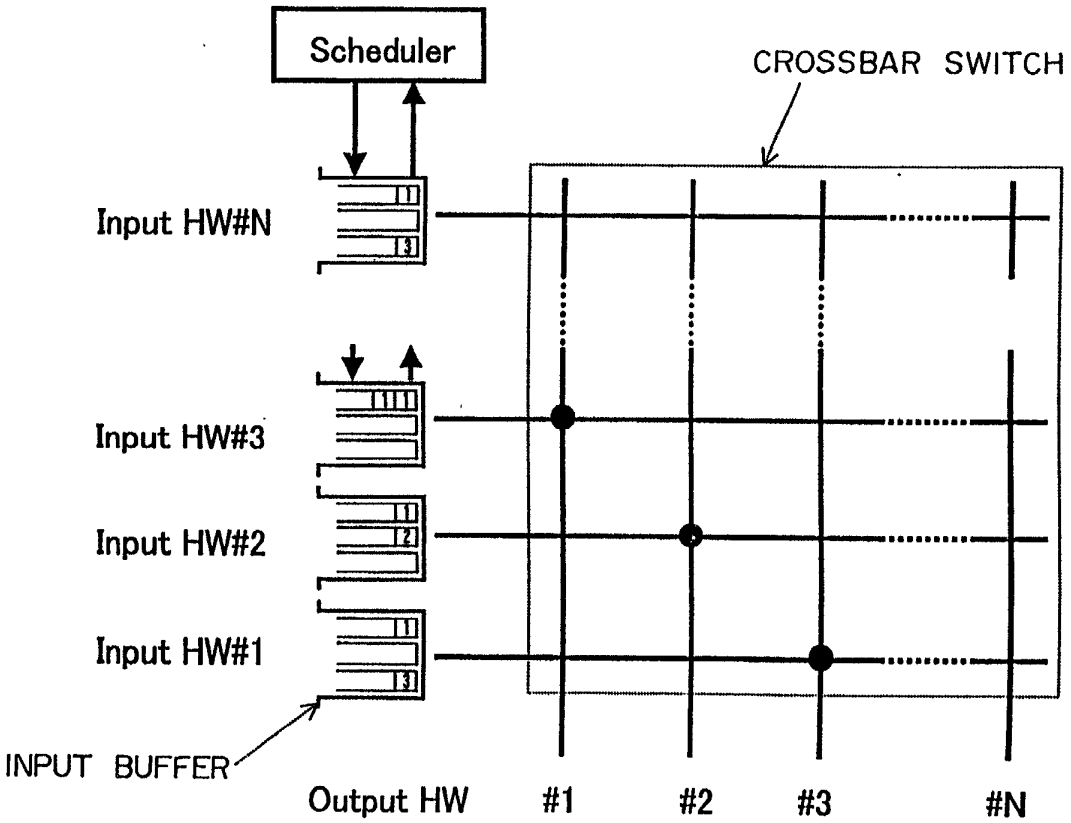


FIG. 1 PRIOR ART

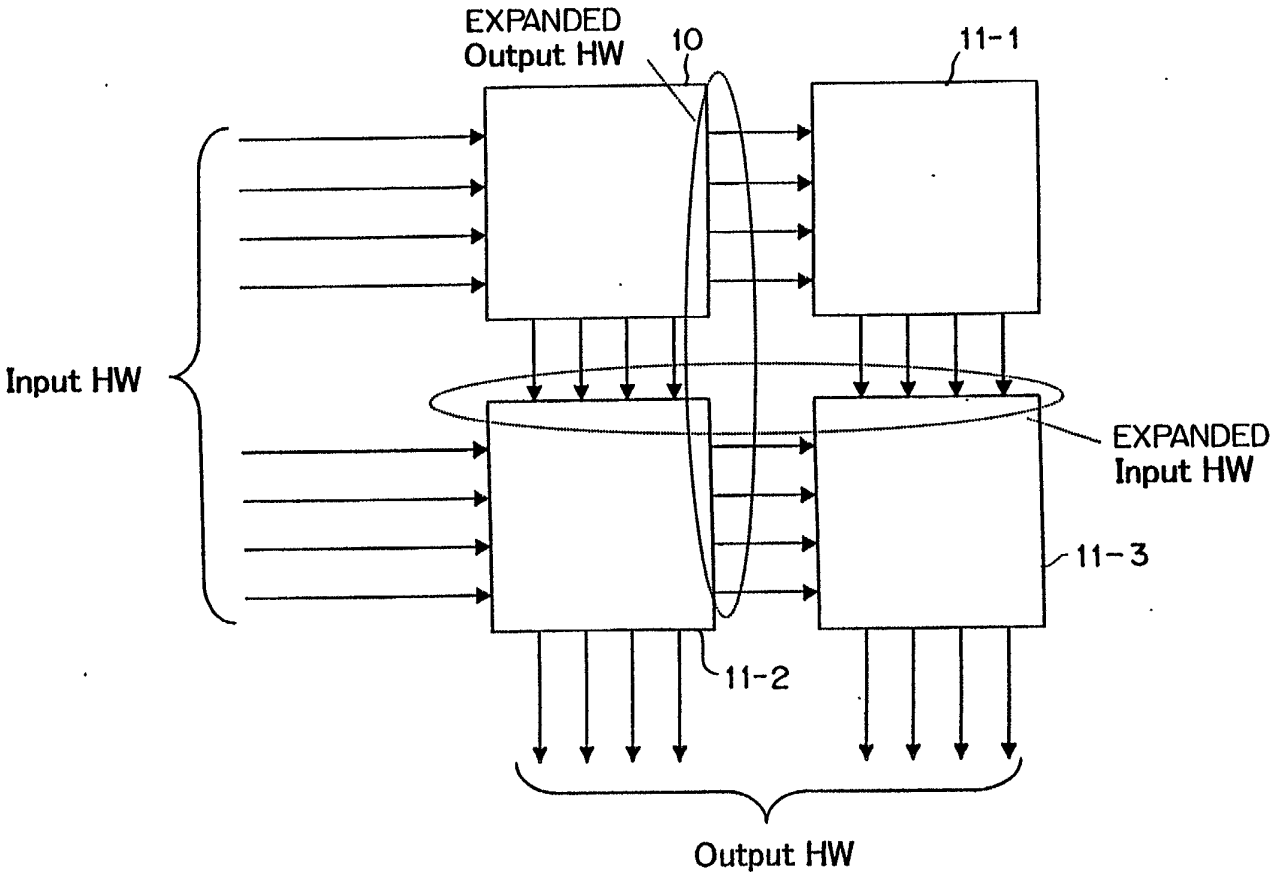


FIG. 2 PRIOR ART

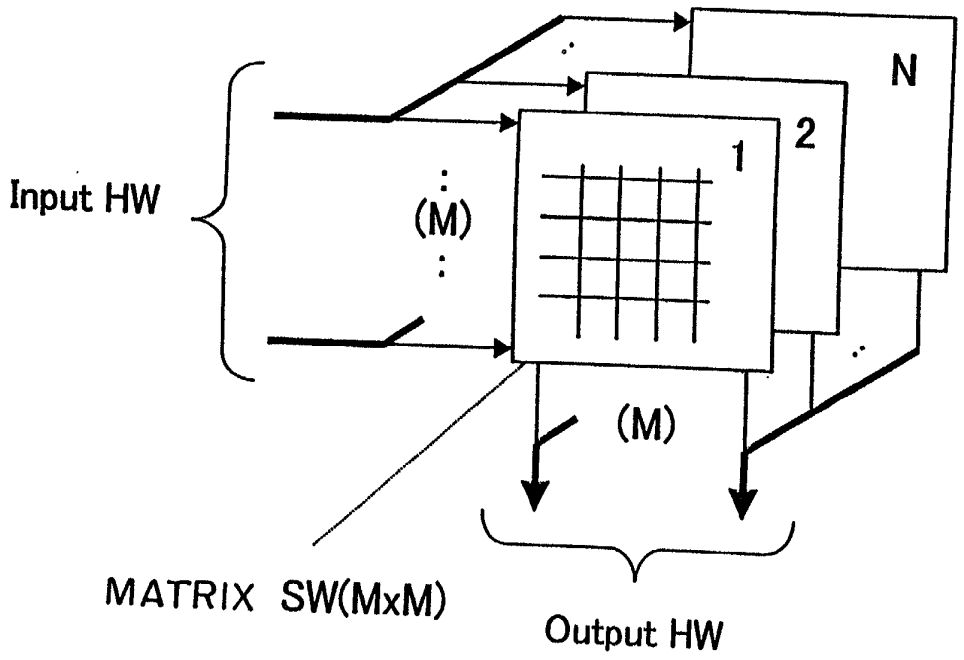


FIG. 3 PRIOR ART

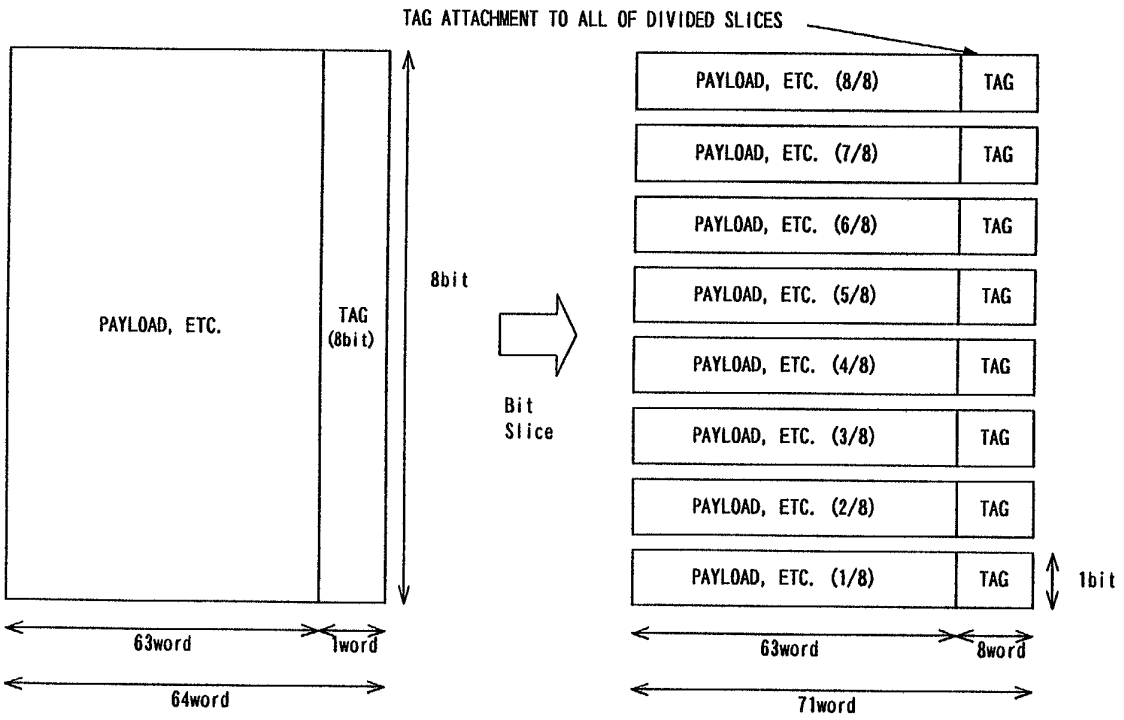


FIG. 4 PRIOR ART

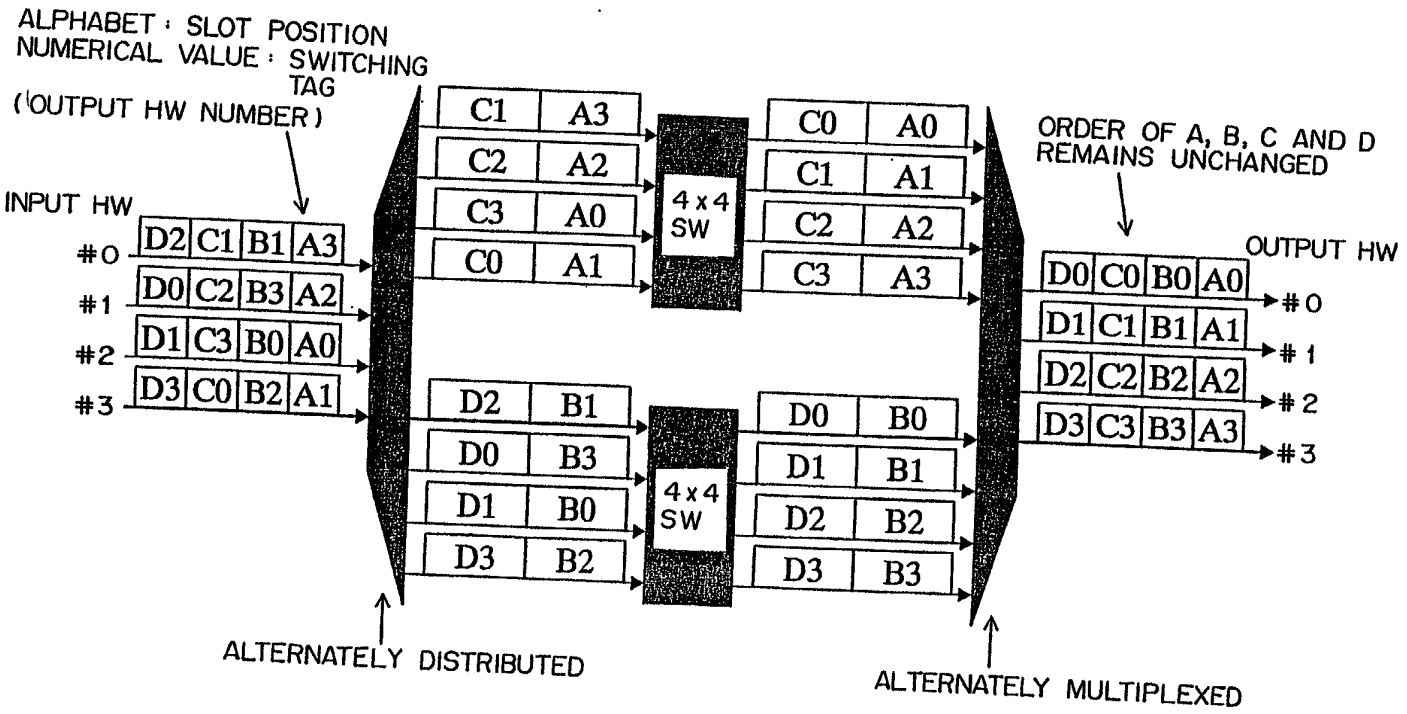

ALPHABET : SLOT POSITION
NUMERICAL VALUE : SWITCHING TAG
(OUTPUT HW NUMBER)
INPUT HW
#0
#1
#2
#3
D2 C1 B1 A3
D0 C2 B3 A2
D1 C3 B0 A0
D3 C0 B2 A1
C1 A3
C2 A2
C3 A0
C0 A1
4 x 4 SW
D2 B1
D0 B3
D1 B0
D3 B2
4 x 4 SW
C0 A0
C1 A1
C2 A2
C3 A3
D0 B0
D1 B1
D2 B2
D3 B3
ORDER OF A, B, C AND D REMAINS UNCHANGED
OUTPUT HW
D0 C0 B0 A0
D1 C1 B1 A1
D2 C2 B2 A2
D3 C3 B3 A3
#0
#1
#2
#3
ALTERNATELY DISTRIBUTED
ALTERNATELY MULTIPLEXED

FIG. 5

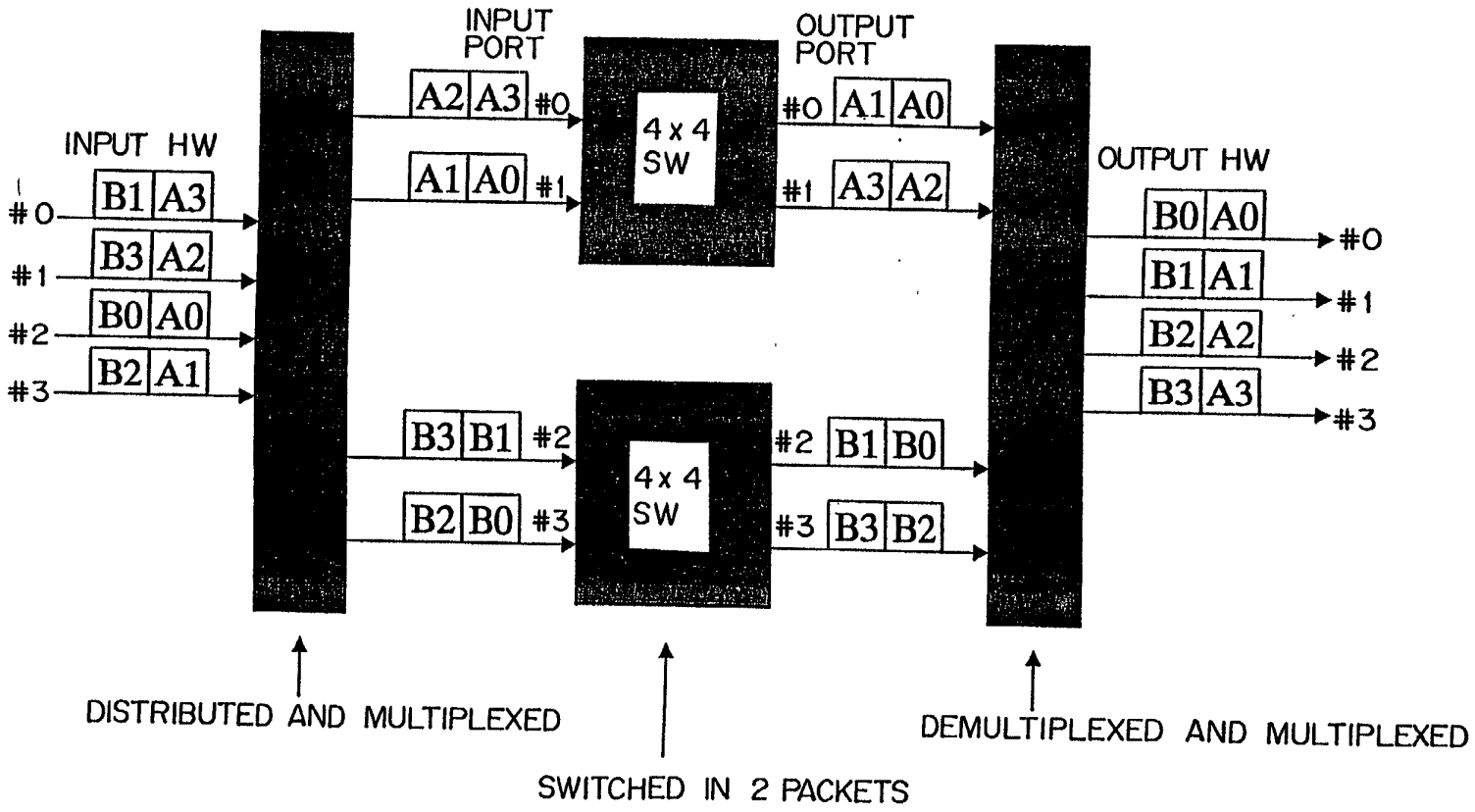

INPUT HW
#0
#1
#2
#3
B1 A3
B3 A2
B0 A0
B2 A1
INPUT PORT
A2 A3 #0
A1 A0 #1
B3 B1 #2
B2 B0 #3
4 x 4 SW
4 x 4 SW
OUTPUT PORT
#0 A1 A0
#1 A3 A2
#2 B1 B0
#3 B3 B2
OUTPUT HW
B0 A0 #0
B1 A1 #1
B2 A2 #2
B3 A3 #3
DISTRIBUTED AND MULTIPLEXED
SWITCHED IN 2 PACKETS
DEMULTIPLEXED AND MULTIPLEXED

FIG. 6

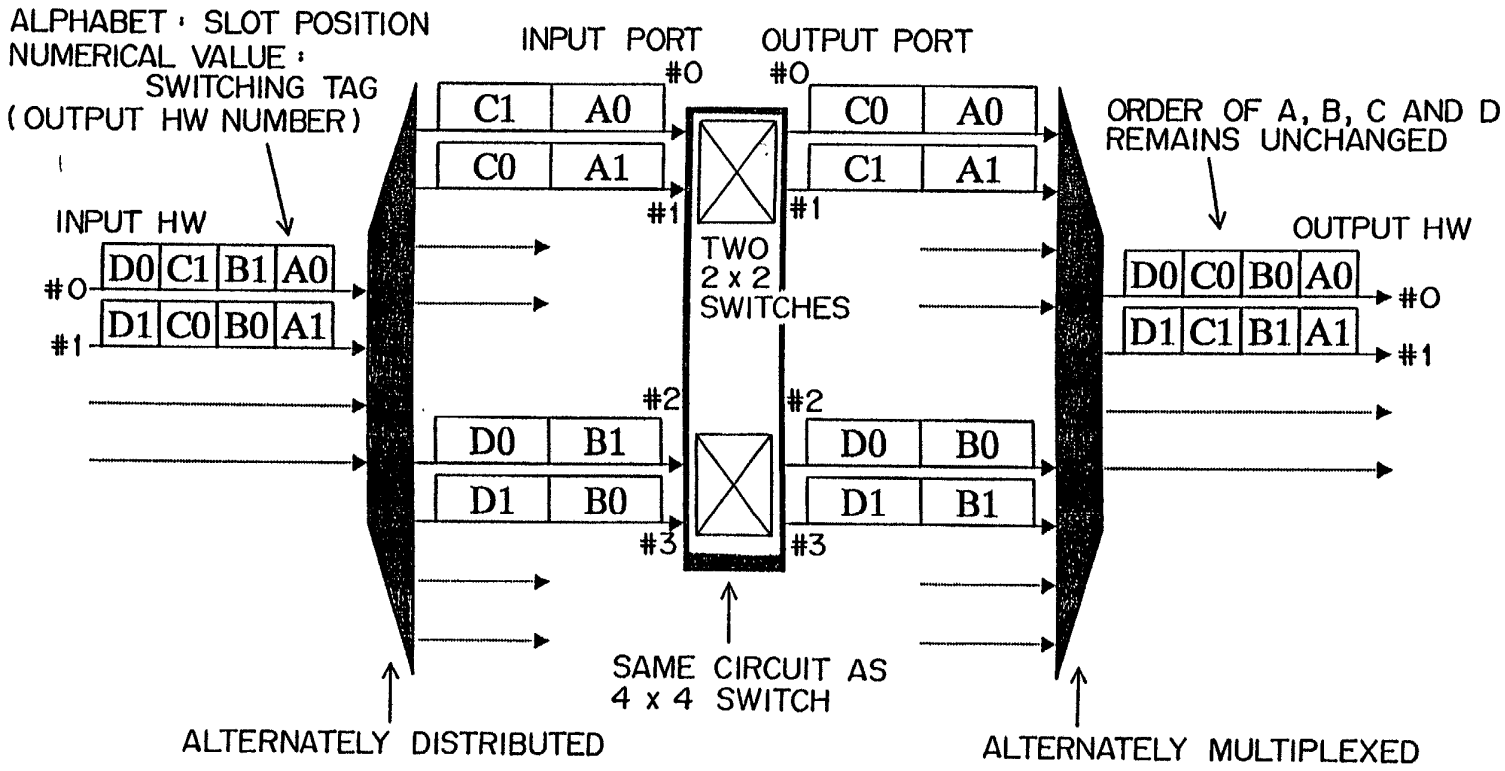

ALPHABET : SLOT POSITION
NUMERICAL VALUE :
SWITCHING TAG
(OUTPUT HW NUMBER)
INPUT PORT
OUTPUT PORT
#0
#0
C1 A0
C0 A1
C0 A0
C1 A1
#1
#1
ORDER OF A, B, C AND D
REMAINS UNCHANGED
INPUT HW
OUTPUT HW
#0
D0 C1 B1 A0
D0 C0 B0 A0
#0
#1
D1 C0 B0 A1
D1 C1 B1 A1
#1
TWO
2 x 2
SWITCHES
#2
#2
D0 B1
D0 B0
D1 B0
D1 B1
#3
#3
SAME CIRCUIT AS
4 x 4 SWITCH
ALTERNATELY DISTRIBUTED
ALTERNATELY MULTIPLEXED

FIG. 7

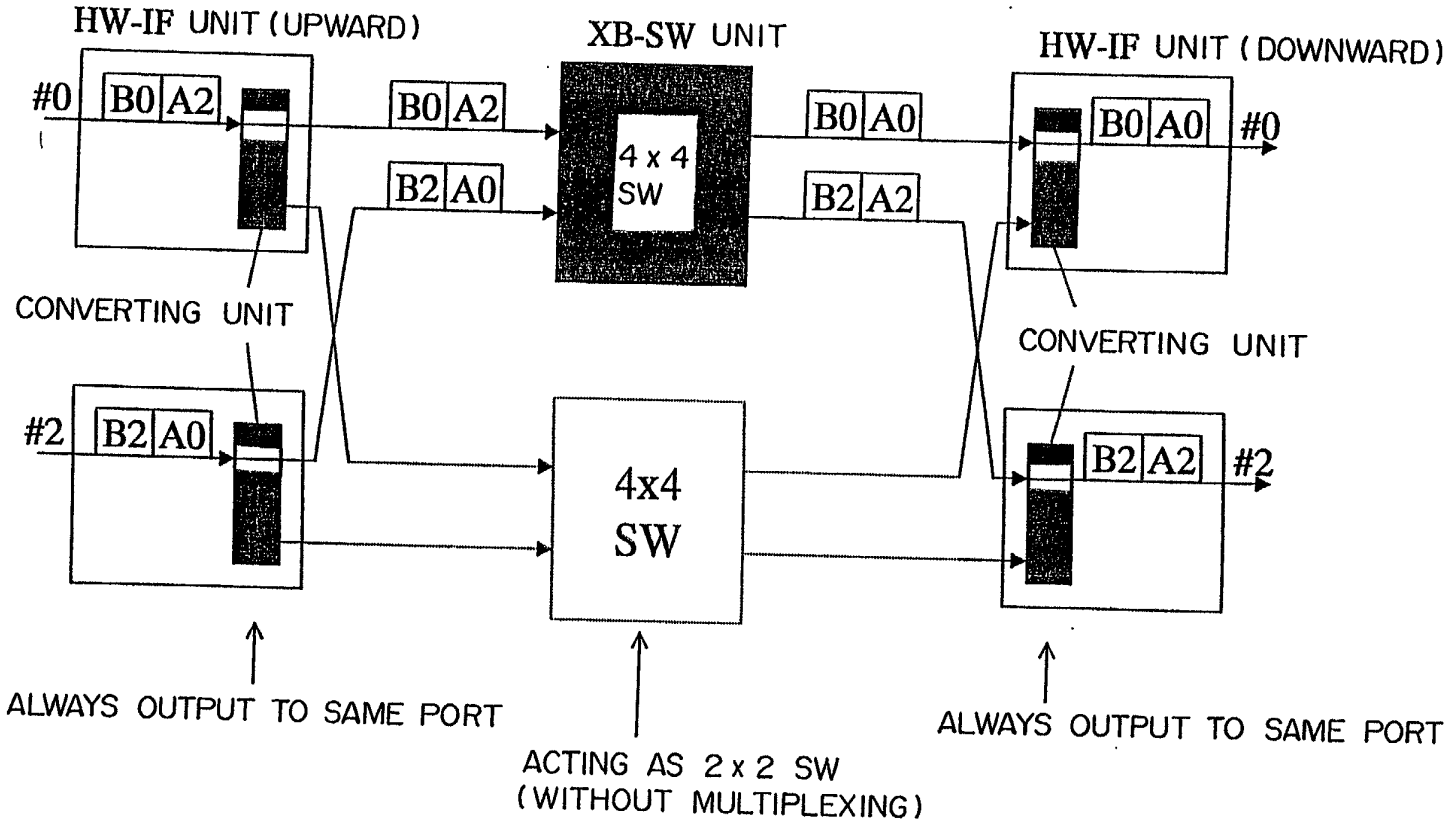

HW-IF UNIT (UPWARD)
XB-SW UNIT
HW-IF UNIT (DOWNWARD)
#0
B0 A2
B0 A2
B2 A0
4 x 4
SW
B0 A0
B2 A2
B0 A0
#0
CONVERTING UNIT
CONVERTING UNIT
#2
B2 A0
4x4
SW
B2 A2
#2
ALWAYS OUTPUT TO SAME PORT
ACTING AS 2 x 2 SW
(WITHOUT MULTIPLEXING)
ALWAYS OUTPUT TO SAME PORT

FIG. 8

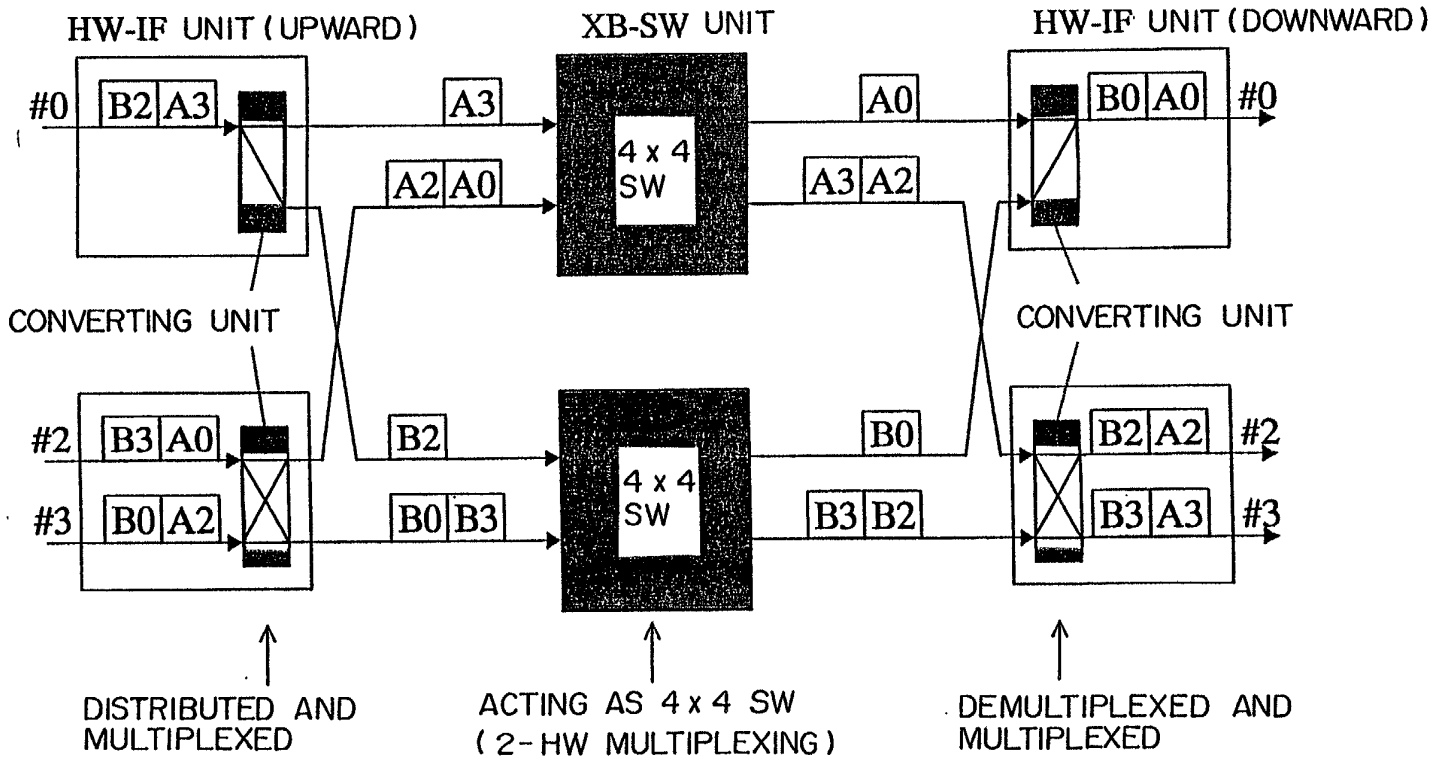

HW-IF UNIT (UPWARD)
XB-SW UNIT
HW-IF UNIT (DOWNWARD)
#0
B2 A3
A3
A2 A0
4 x 4 SW
A0
A3 A2
B0 A0
#0
CONVERTING UNIT
CONVERTING UNIT
#2
B3 A0
#3
B0 A2
B2
B0 B3
4 x 4 SW
B0
B3 B2
B2 A2
#2
B3 A3
#3
DISTRIBUTED AND MULTIPLEXED
ACTING AS 4 x 4 SW (2-HW MULTIPLEXING)
DEMULTIPLEXED AND MULTIPLEXED

FIG. 9

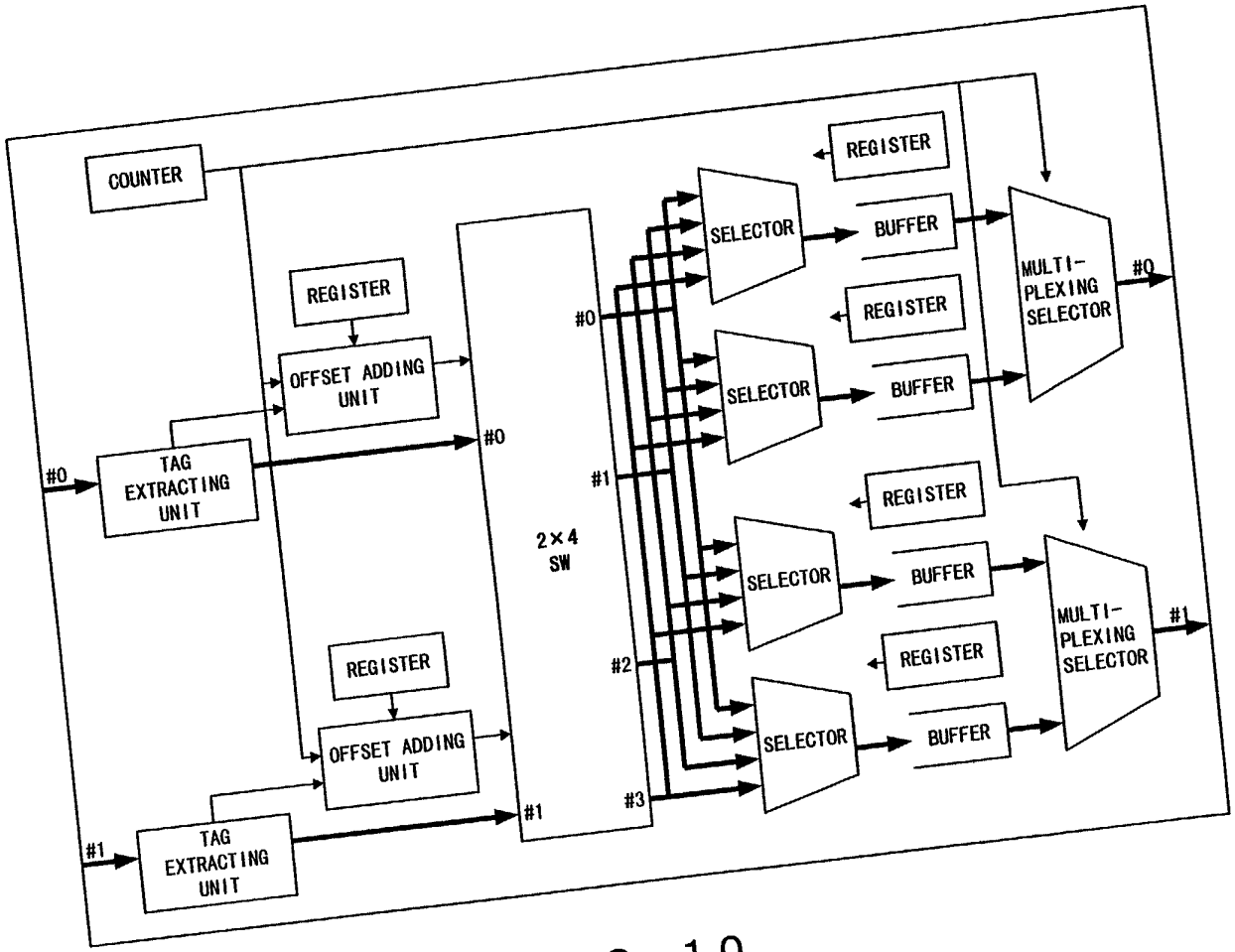


FIG. 10

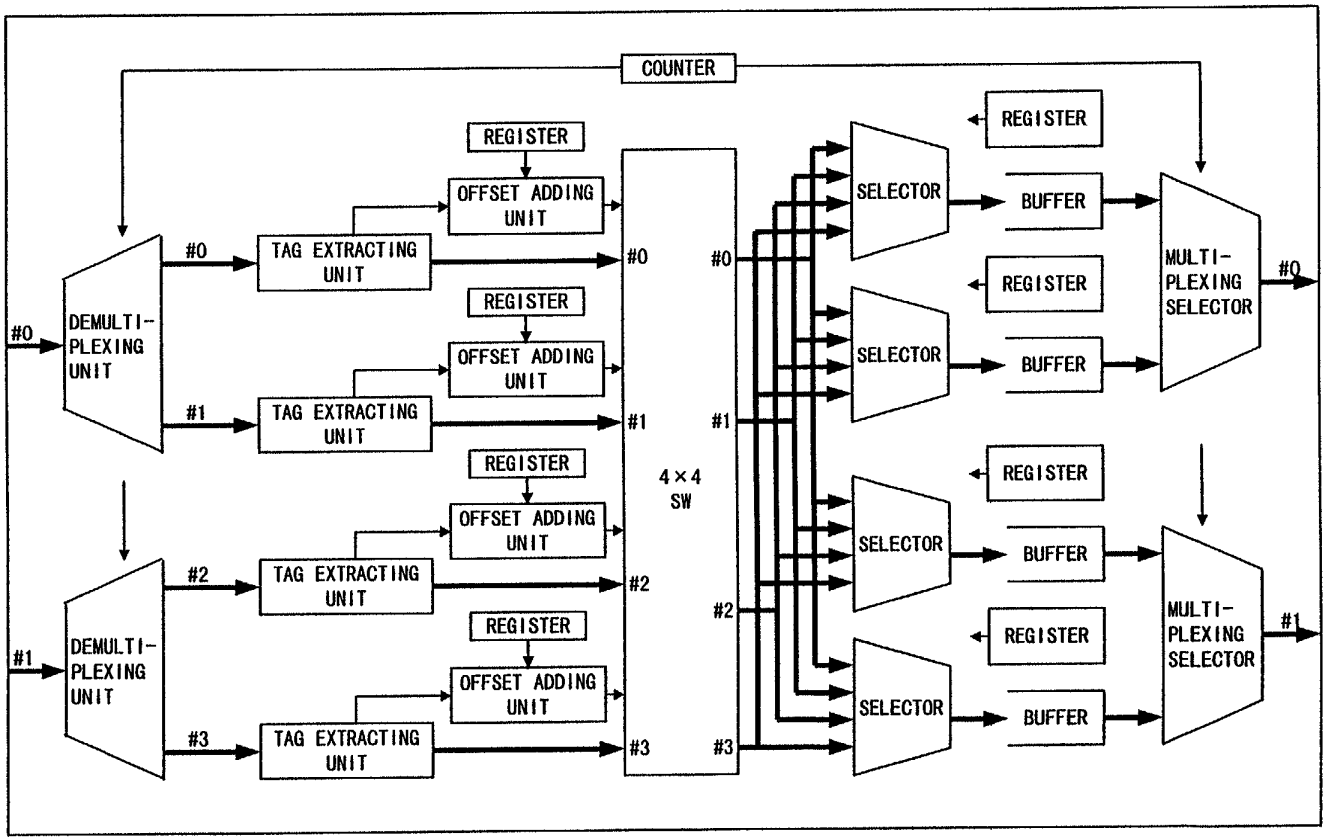

COUNTER
REGISTER
OFFSET ADDING UNIT
TAG EXTRACTING UNIT
#0
#1
#2
#3
DEMULTI-PLEXING UNIT
4×4 SW
SELECTOR
BUFFER
MULTI-PLEXING SELECTOR

FIG. 11

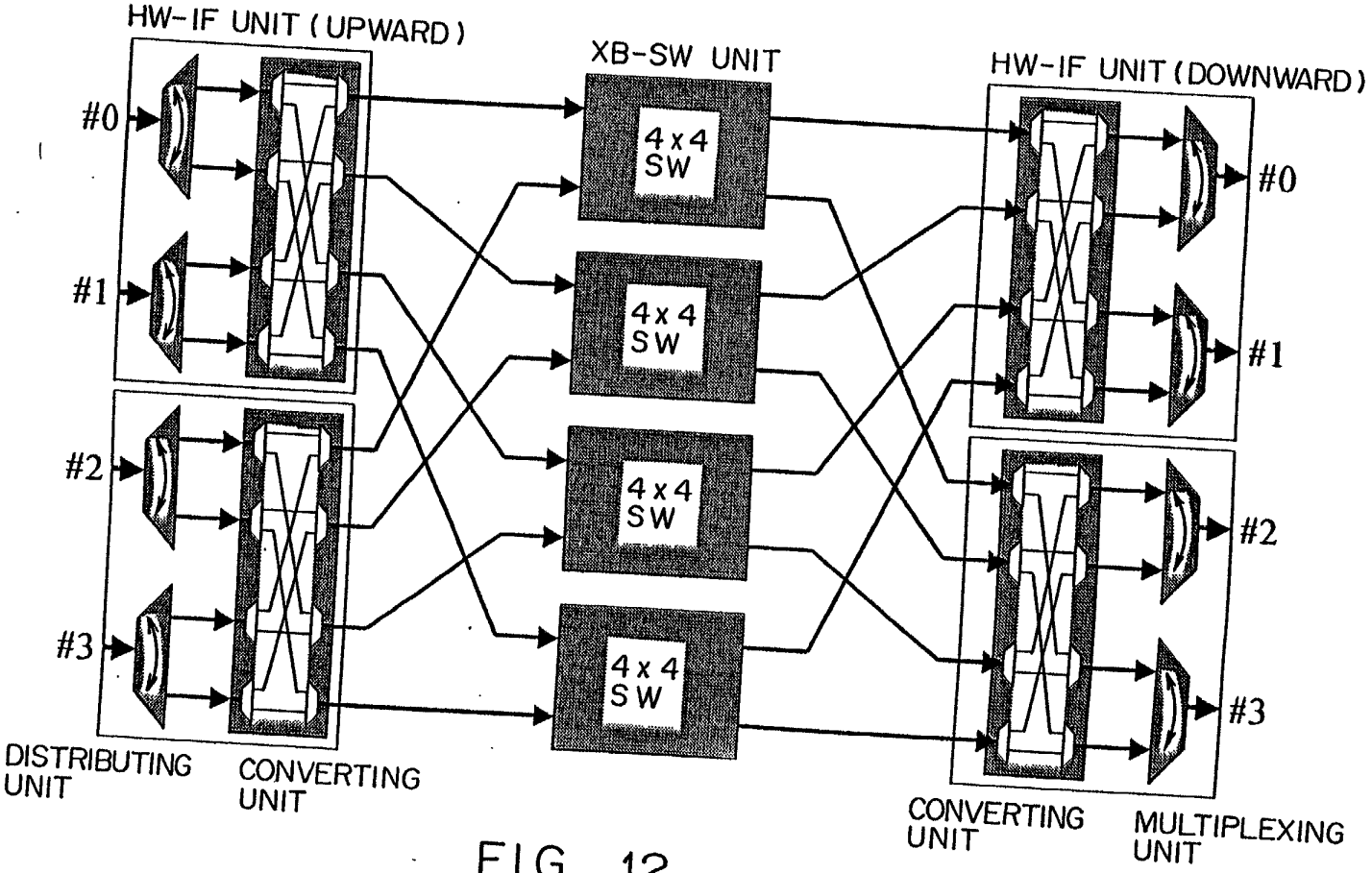


FIG. 12

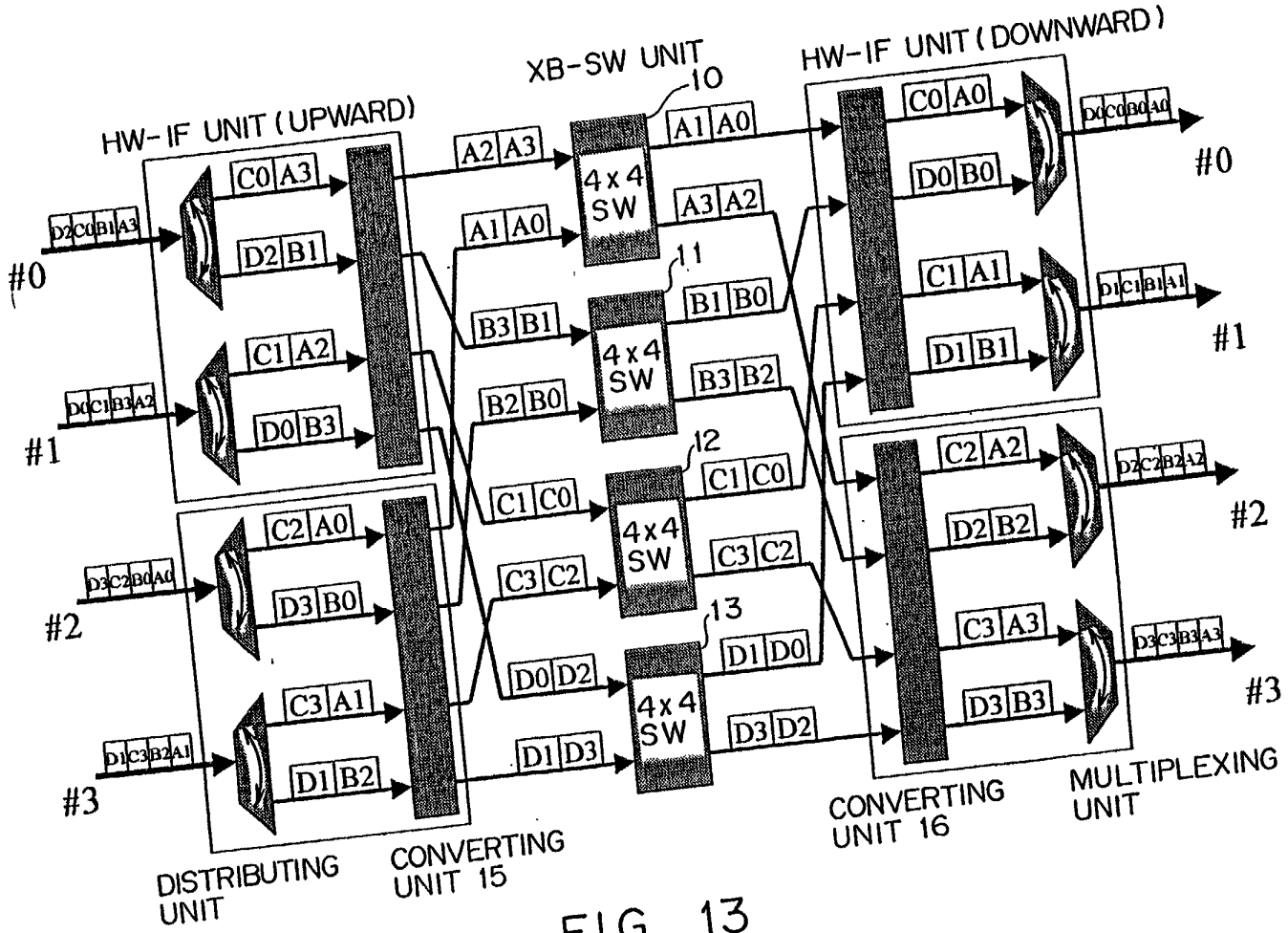

HW-IF UNIT (UPWARD)
XB-SW UNIT
10
HW-IF UNIT (DOWNWARD)
4x4 SW
11
12
13
#0
#1
#2
#3
DISTRIBUTING UNIT
CONVERTING UNIT 15
CONVERTING UNIT 16
MULTIPLEXING UNIT

FIG. 13

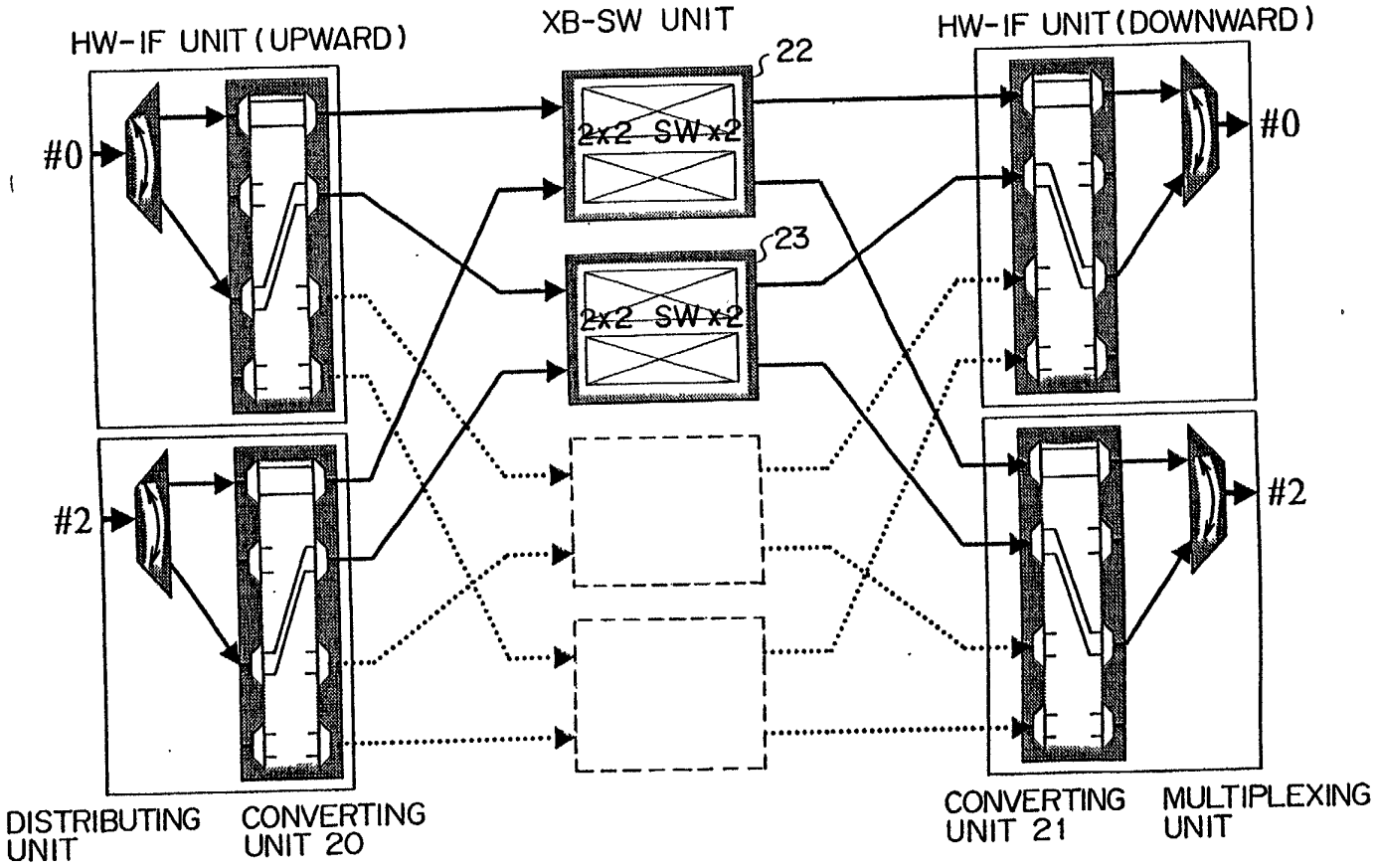

HW-IF UNIT(UPWARD)
XB-SW UNIT
HW-IF UNIT(DOWNWARD)
22
2x2 SW x2
23
2x2 SW x2
#0
#2
#0
#2
DISTRIBUTING UNIT
CONVERTING UNIT 20
CONVERTING UNIT 21
MULTIPLEXING UNIT

FIG. 14

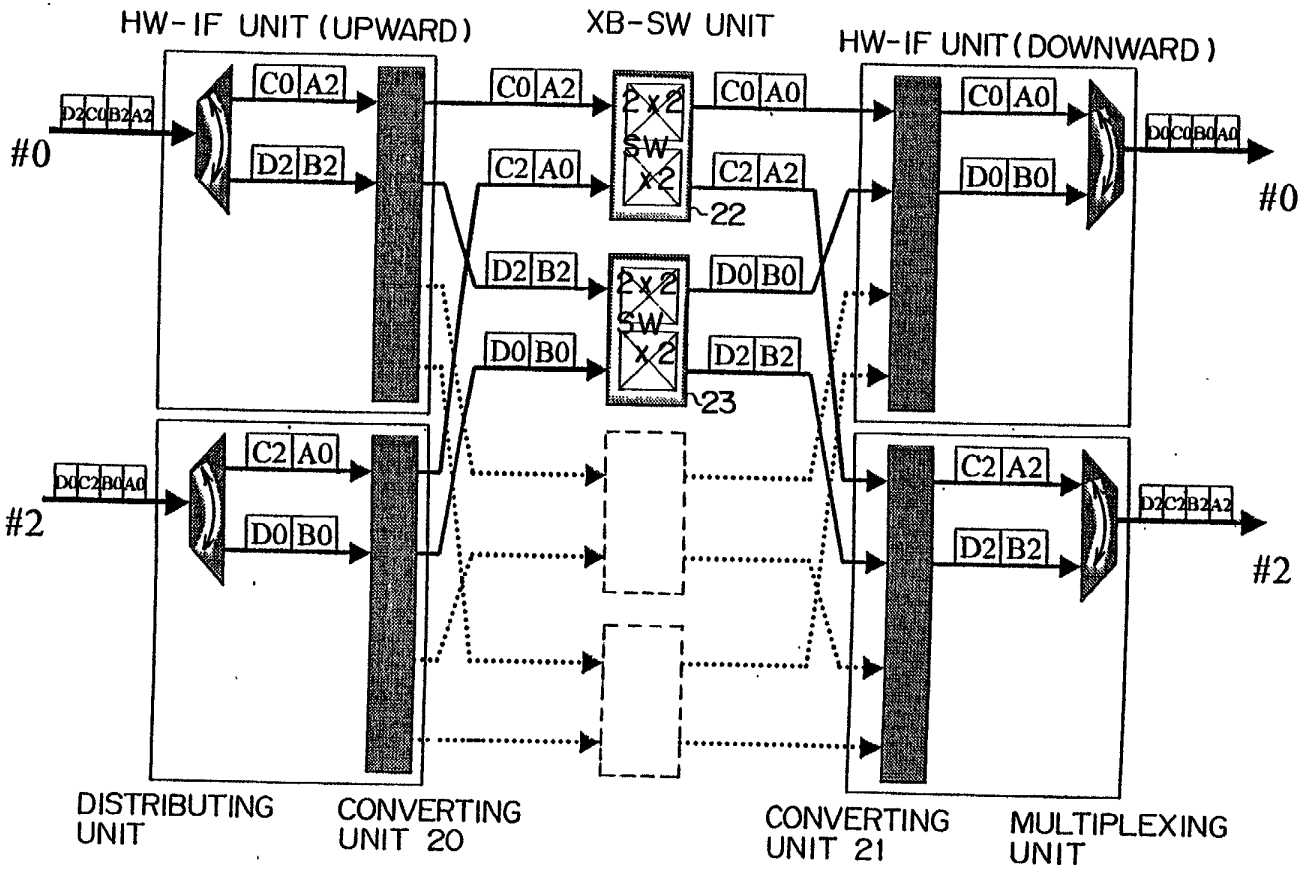

HW-IF UNIT (UPWARD)
XB-SW UNIT
HW-IF UNIT (DOWNWARD)
D2C0B2A2
#0
C0 A2
D2 B2
C0 A2
C2 A0
D2 B2
D0 B0
2x2 SW x2
22
23
C0 A0
C2 A2
D0 B0
D2 B2
D0C0B0A0
#0
D0C2B0A0
#2
C2 A0
D0 B0
C2 A2
D2 B2
D2C2B2A2
#2
DISTRIBUTING UNIT
CONVERTING UNIT 20
CONVERTING UNIT 21
MULTIPLEXING UNIT

FIG. 15

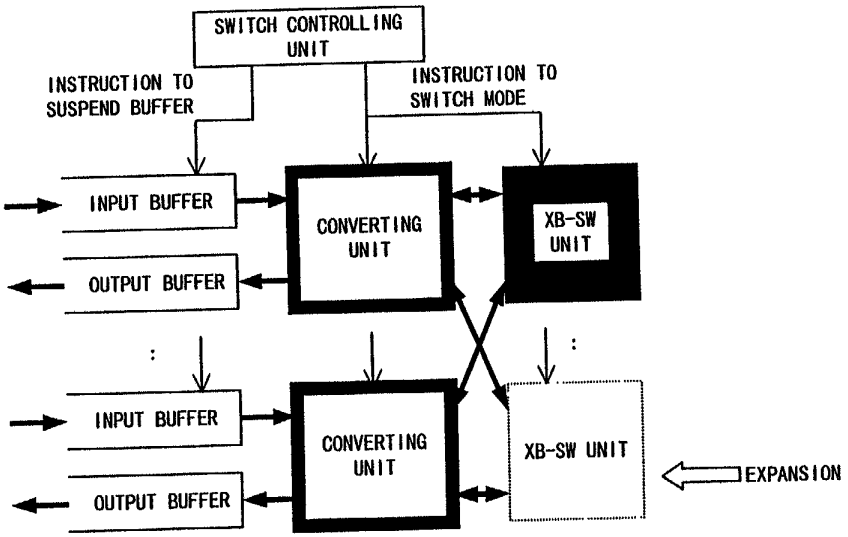

SWITCH CONTROLLING UNIT
INSTRUCTION TO SUSPEND BUFFER
INSTRUCTION TO SWITCH MODE
INPUT BUFFER
OUTPUT BUFFER
CONVERTING UNIT
XB-SW UNIT
INPUT BUFFER
OUTPUT BUFFER
CONVERTING UNIT
XB-SW UNIT
EXPANSION

FIG. 16

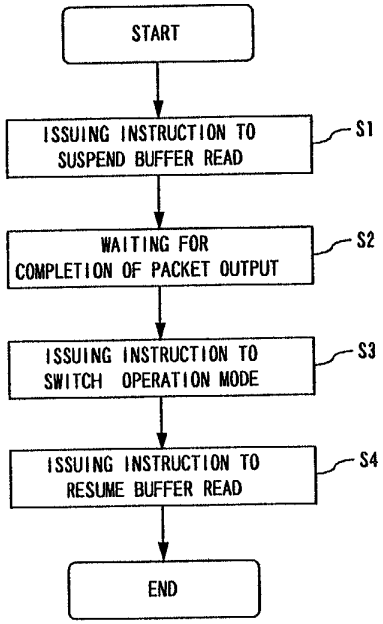

START
ISSUING INSTRUCTION TO SUSPEND BUFFER READ
S1
WAITING FOR COMPLETION OF PACKET OUTPUT
S2
ISSUING INSTRUCTION TO SWITCH OPERATION MODE
S3
ISSUING INSTRUCTION TO RESUME BUFFER READ
S4
END

FIG. 17

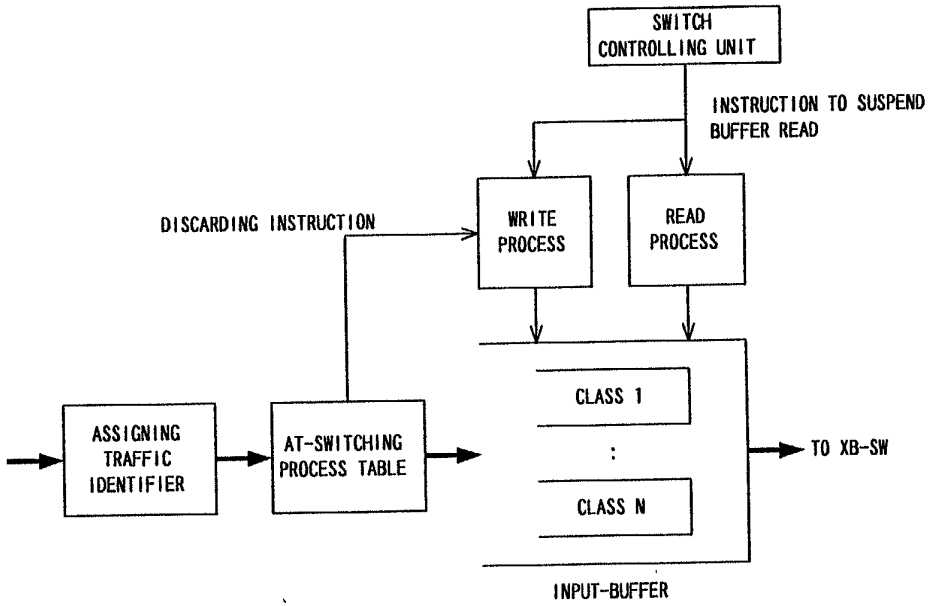

SWITCH CONTROLLING UNIT
INSTRUCTION TO SUSPEND BUFFER READ
DISCARDING INSTRUCTION
WRITE PROCESS
READ PROCESS
ASSIGNING TRAFFIC IDENTIFIER
AT-SWITCHING PROCESS TABLE
CLASS 1
:
CLASS N
TO XB-SW
INPUT-BUFFER

FIG. 18

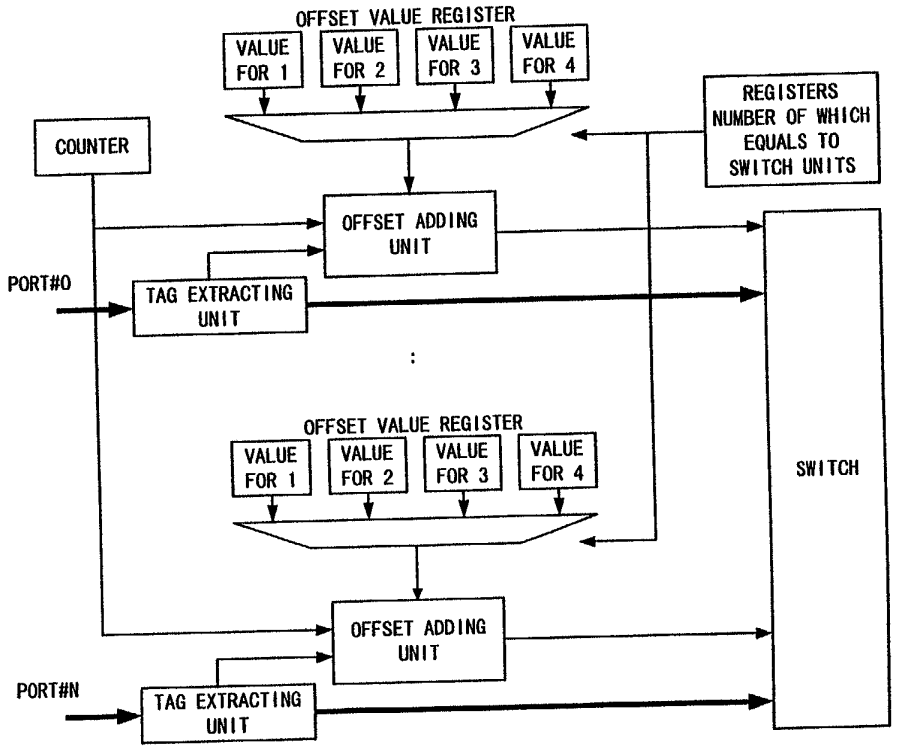

OFFSET VALUE REGISTER
VALUE FOR 1
VALUE FOR 2
VALUE FOR 3
VALUE FOR 4
REGISTERS NUMBER OF WHICH EQUALS TO SWITCH UNITS
COUNTER
OFFSET ADDING UNIT
PORT#0
TAG EXTRACTING UNIT
:
OFFSET VALUE REGISTER
VALUE FOR 1
VALUE FOR 2
VALUE FOR 3
VALUE FOR 4
SWITCH
OFFSET ADDING UNIT
PORT#N
TAG EXTRACTING UNIT

FIG. 19

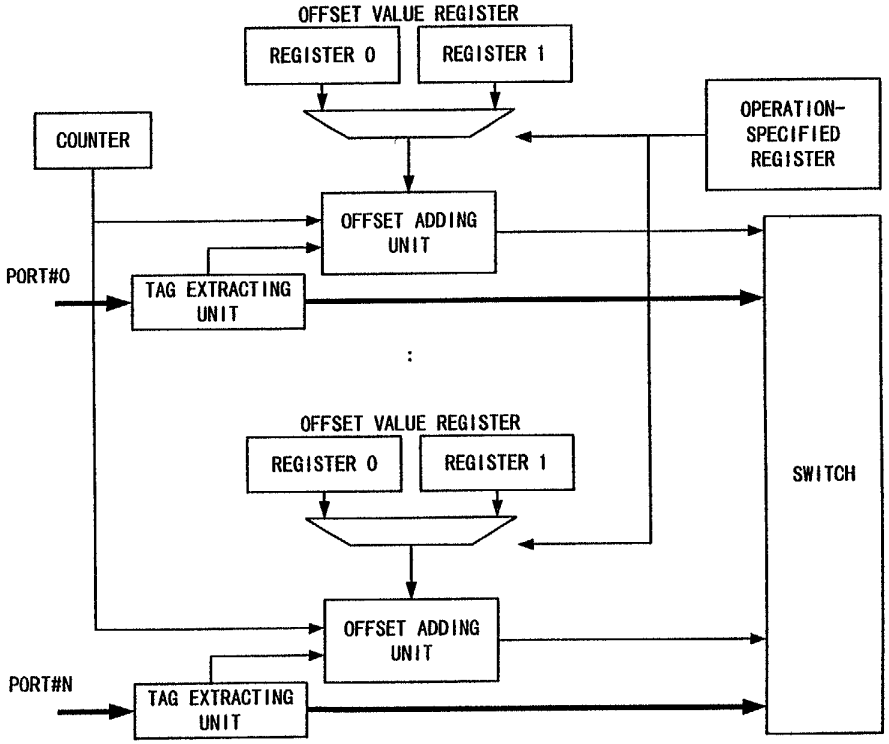

OFFSET VALUE REGISTER
REGISTER 0
REGISTER 1
OPERATION-SPECIFIED REGISTER
COUNTER
OFFSET ADDING UNIT
PORT#0
TAG EXTRACTING UNIT
:
OFFSET VALUE REGISTER
REGISTER 0
REGISTER 1
SWITCH
OFFSET ADDING UNIT
PORT#N
TAG EXTRACTING UNIT

FIG. 20

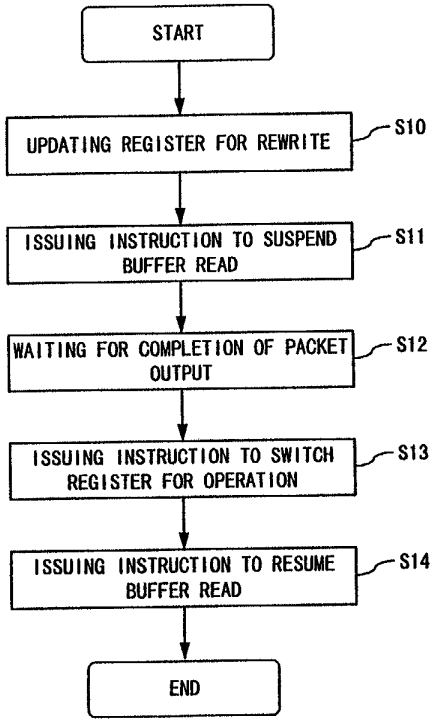

START
UPDATING REGISTER FOR REWRITE
S10
ISSUING INSTRUCTION TO SUSPEND BUFFER READ
S11
WAITING FOR COMPLETION OF PACKET OUTPUT
S12
ISSUING INSTRUCTION TO SWITCH REGISTER FOR OPERATION
S13
ISSUING INSTRUCTION TO RESUME BUFFER READ
S14
END

FIG. 21

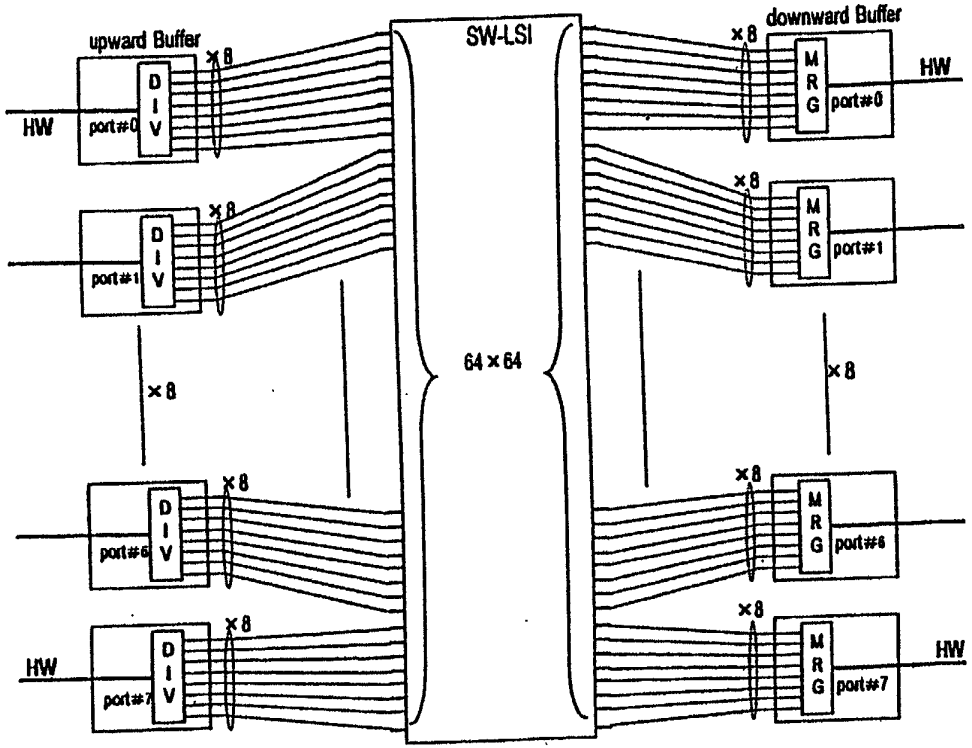

upward Buffer
SW-LSI
downward Buffer
HW
port#0
port#1
port#6
port#7
DIV
MRG
×8
64×64

FIG. 22

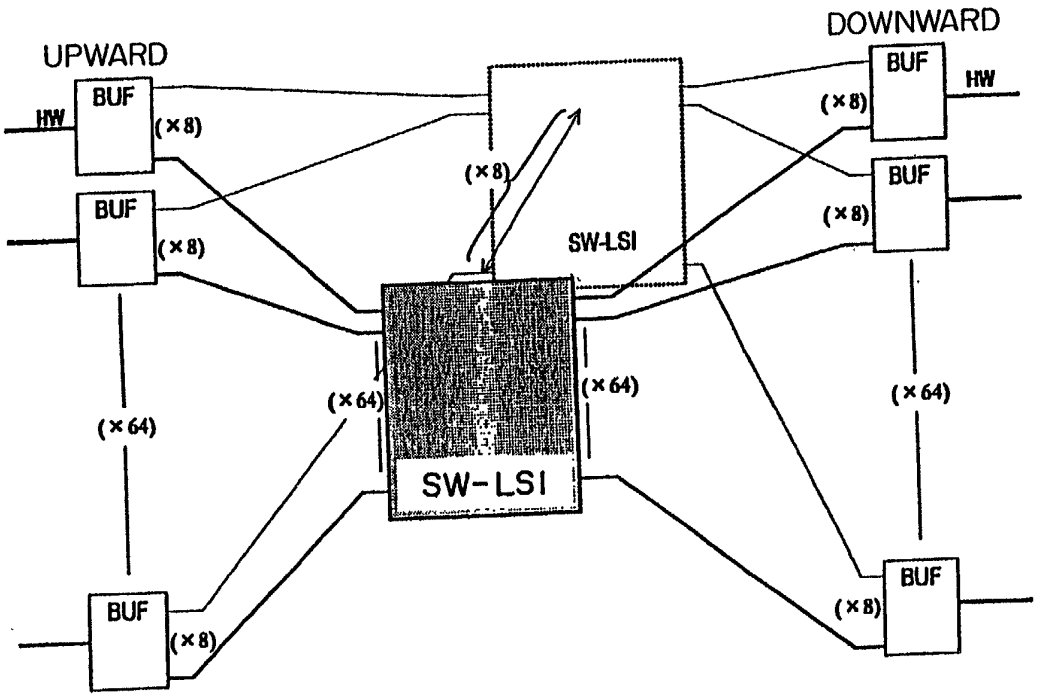


FIG. 23

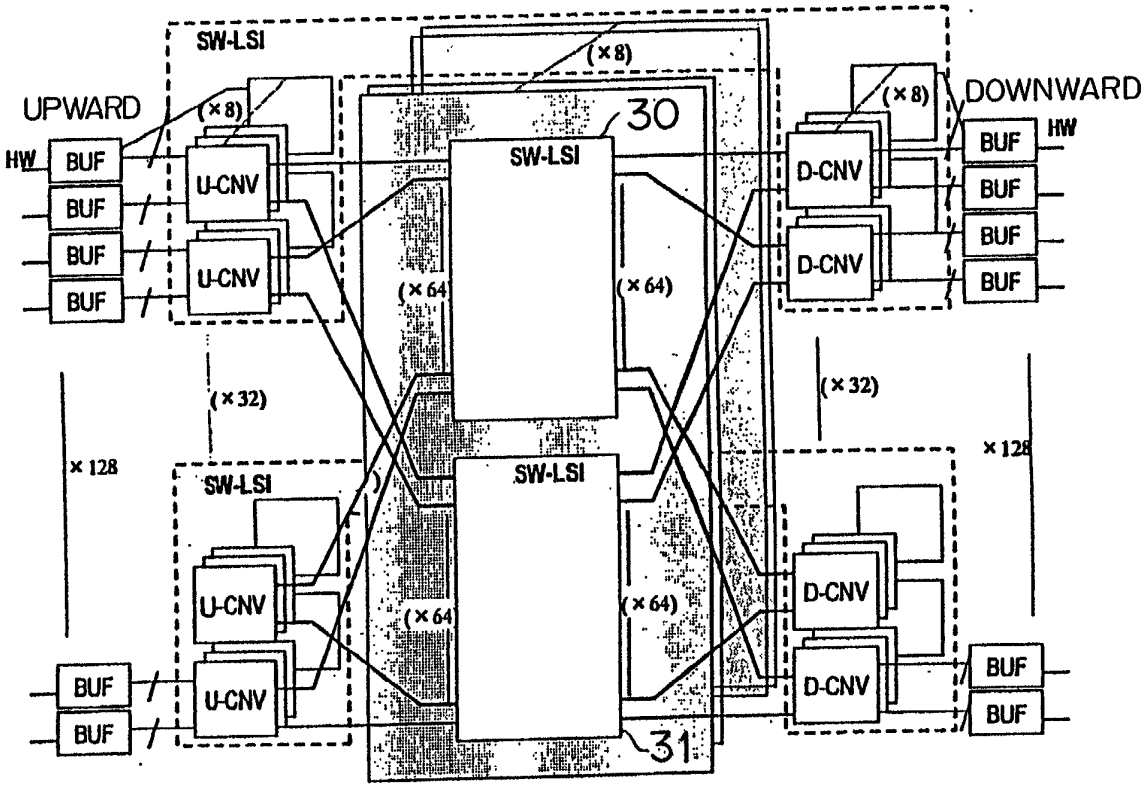

SW-LSI
(×8)
UPWARD
(×8)
30
DOWNWARD
HW
BUF
U-CNV
SW-LSI
D-CNV
(×64)
(×32)
×128
SW-LSI
SW-LSI
31

FIG. 24

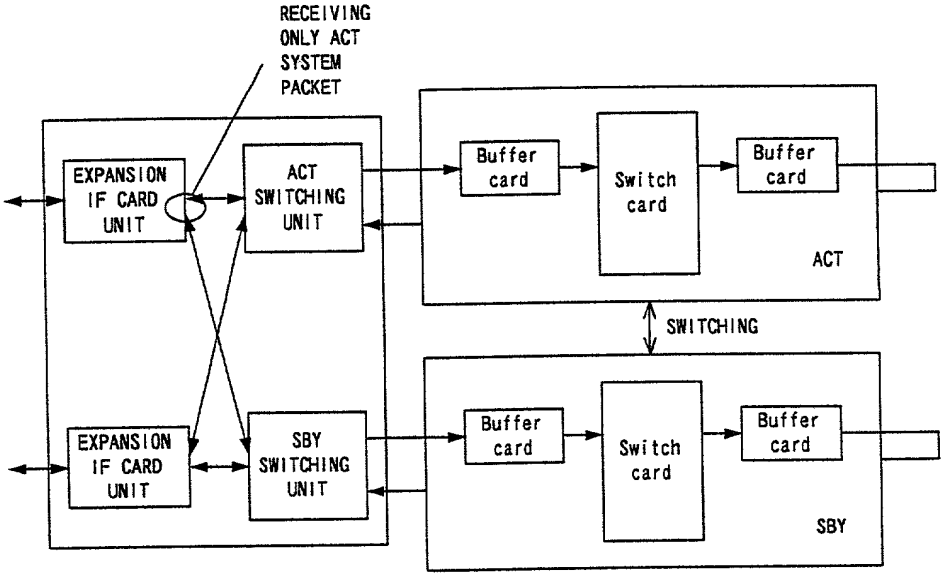

RECEIVING
ONLY ACT
SYSTEM
PACKET
EXPANSION
IF CARD
UNIT
ACT
SWITCHING
UNIT
Buffer
card
Switch
card
Buffer
card
ACT
SWITCHING
EXPANSION
IF CARD
UNIT
SBY
SWITCHING
UNIT
Buffer
card
Switch
card
Buffer
card
SBY

FIG. 25

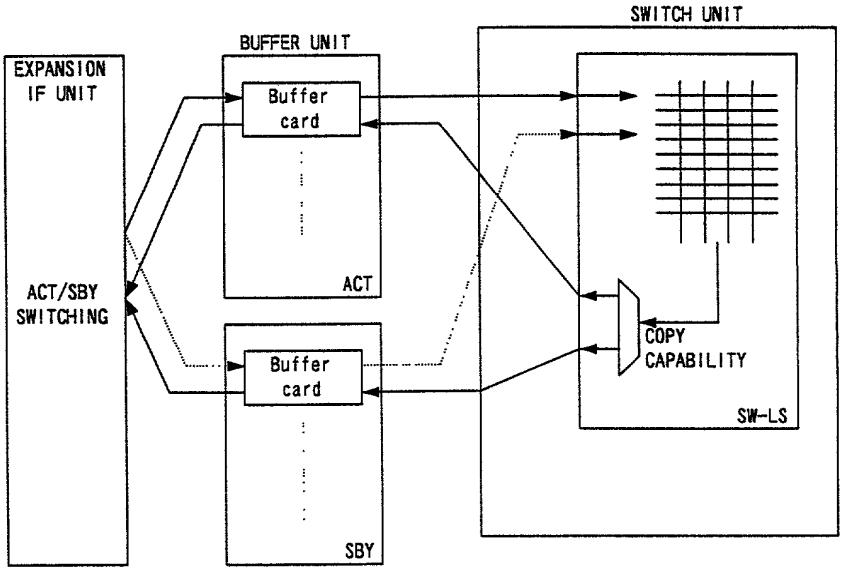

SWITCH UNIT
BUFFER UNIT
EXPANSION
IF UNIT
Buffer
card
ACT
ACT/SBY
SWITCHING
Buffer
card
SBY
COPY
CAPABILITY
SW-LS

FIG. 26

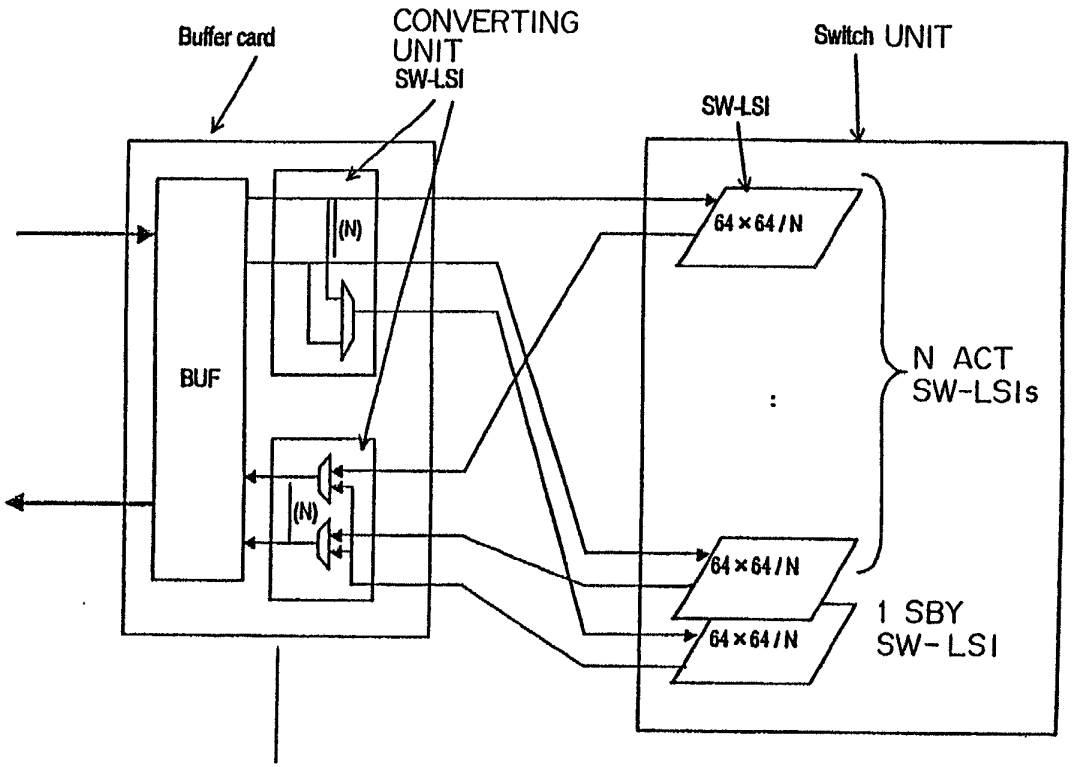


FIG. 27

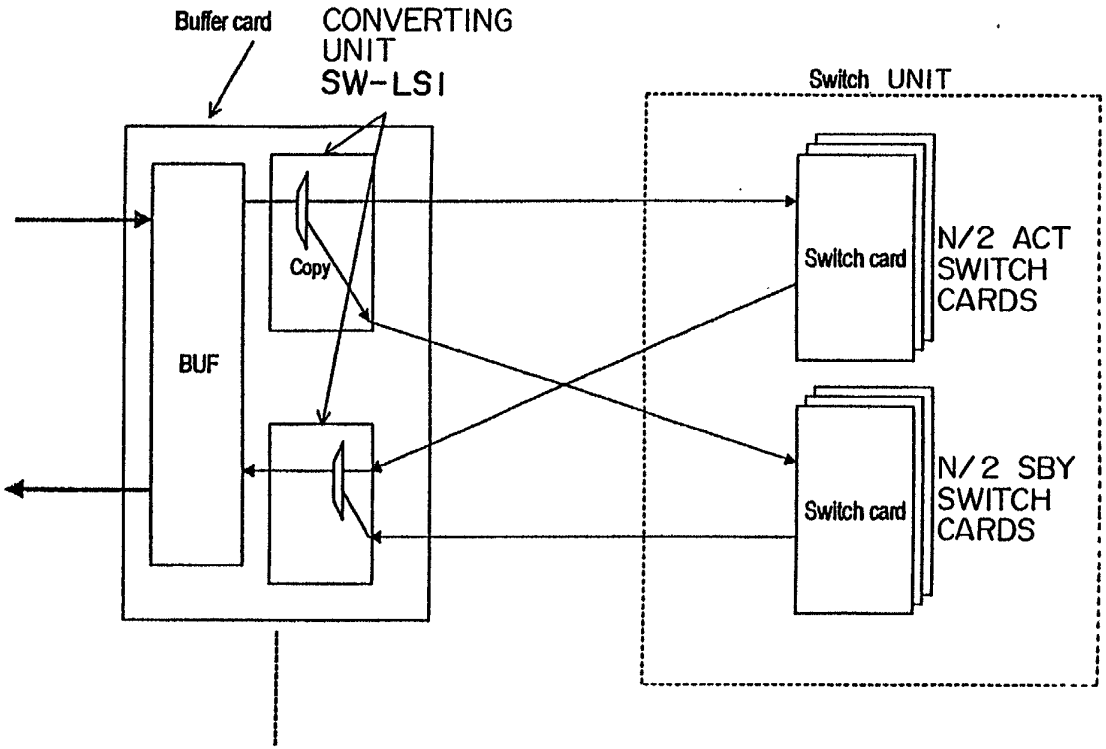

Buffer card
CONVERTING UNIT SW-LSI
Switch UNIT
Copy
BUF
Switch card
N/2 ACT SWITCH CARDS
Switch card
N/2 SBY SWITCH CARDS

FIG. 28

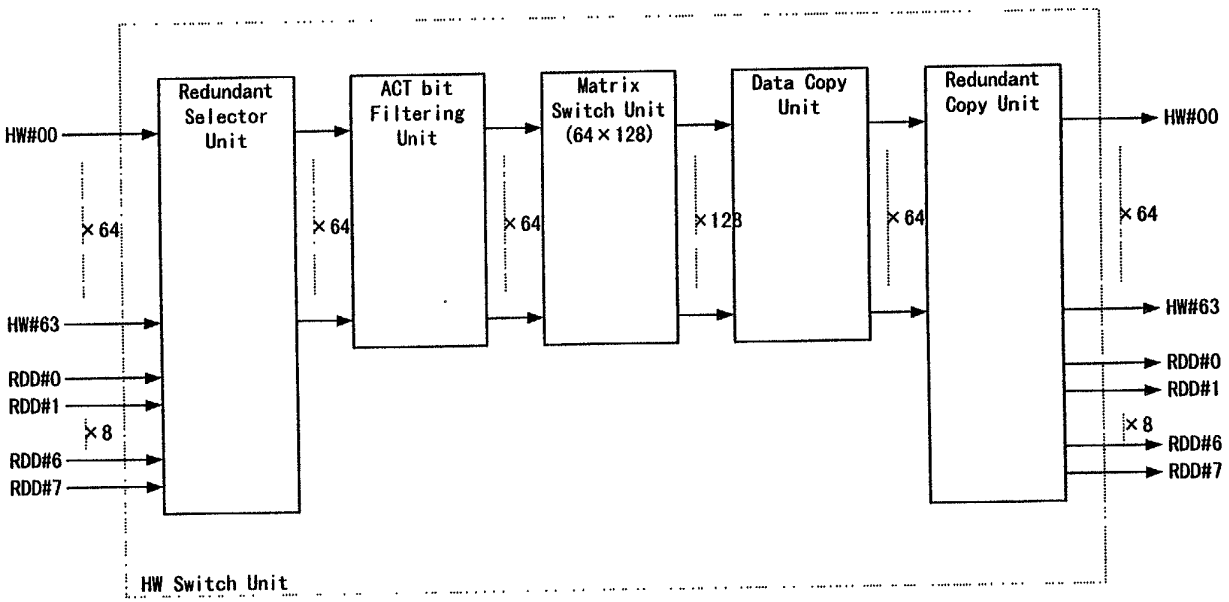

HW#00
×64
HW#63
RDD#0
RDD#1
×8
RDD#6
RDD#7
Redundant Selector Unit
×64
ACT bit Filtering Unit
×64
Matrix Switch Unit (64×128)
×128
Data Copy Unit
×64
Redundant Copy Unit
HW#00
×64
HW#63
RDD#0
RDD#1
×8
RDD#6
RDD#7
HW Switch Unit

FIG. 29

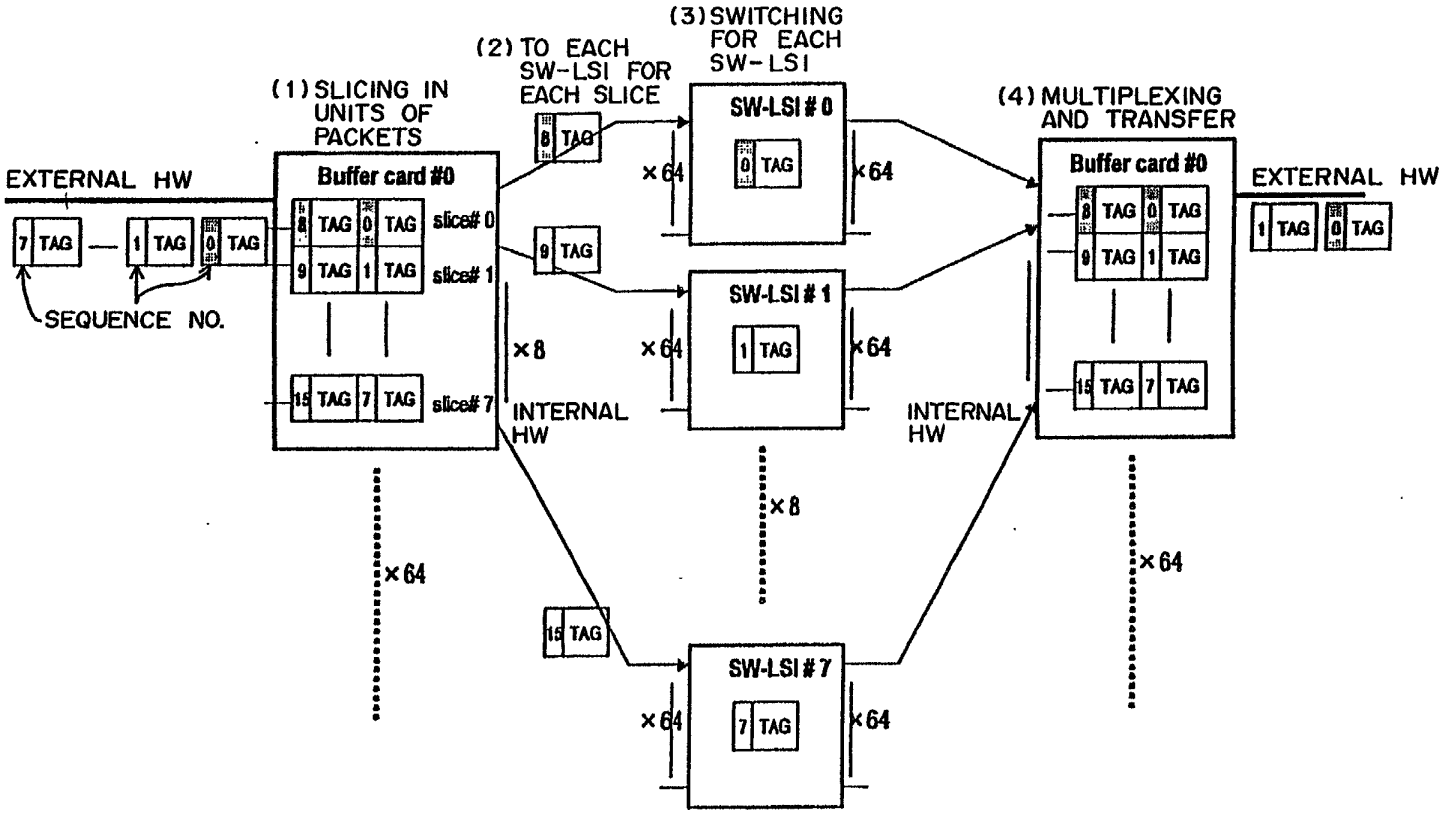
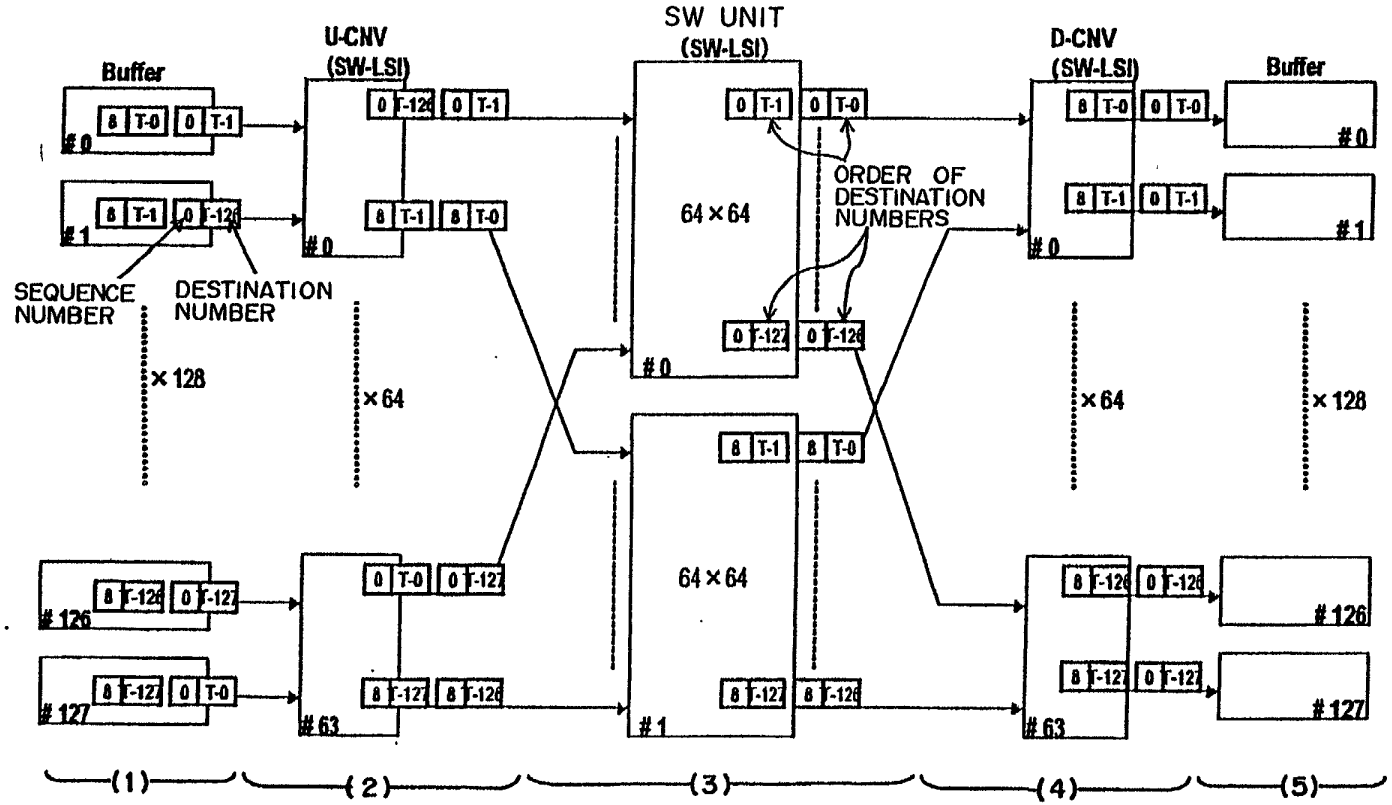

(1) SLICING IN UNITS OF PACKETS
(2) TO EACH SW-LSI FOR EACH SLICE
(3) SWITCHING FOR EACH SW-LSI
(4) MULTIPLEXING AND TRANSFER
EXTERNAL HW
Buffer card #0
SEQUENCE NO.
slice# 0
slice# 1
slice# 7
INTERNAL HW
SW-LSI # 0
SW-LSI # 1
SW-LSI # 7
TAG
×64
×8

FIG. 30



(ONLY FIRST SLICE IS SHOWN)

FIG. 31

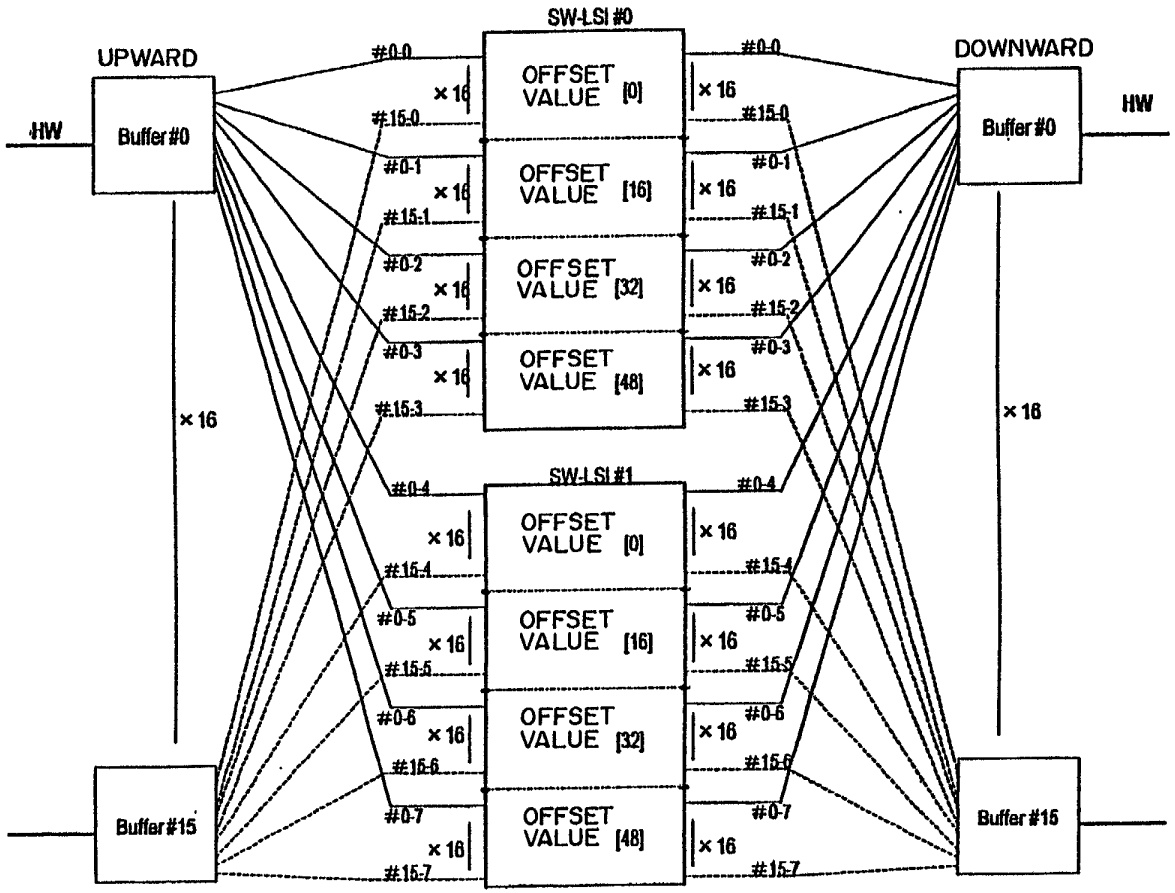

SW-LSI #0
UPWARD
DOWNWARD
HW
Buffer #0
Buffer #15
× 16
OFFSET VALUE [0]
OFFSET VALUE [16]
OFFSET VALUE [32]
OFFSET VALUE [48]
SW-LSI #1
#0-0
#15-0
#0-1
#15-1
#0-2
#15-2
#0-3
#15-3
#0-4
#15-4
#0-5
#15-5
#0-6
#15-6
#0-7
#15-7

FIG. 32

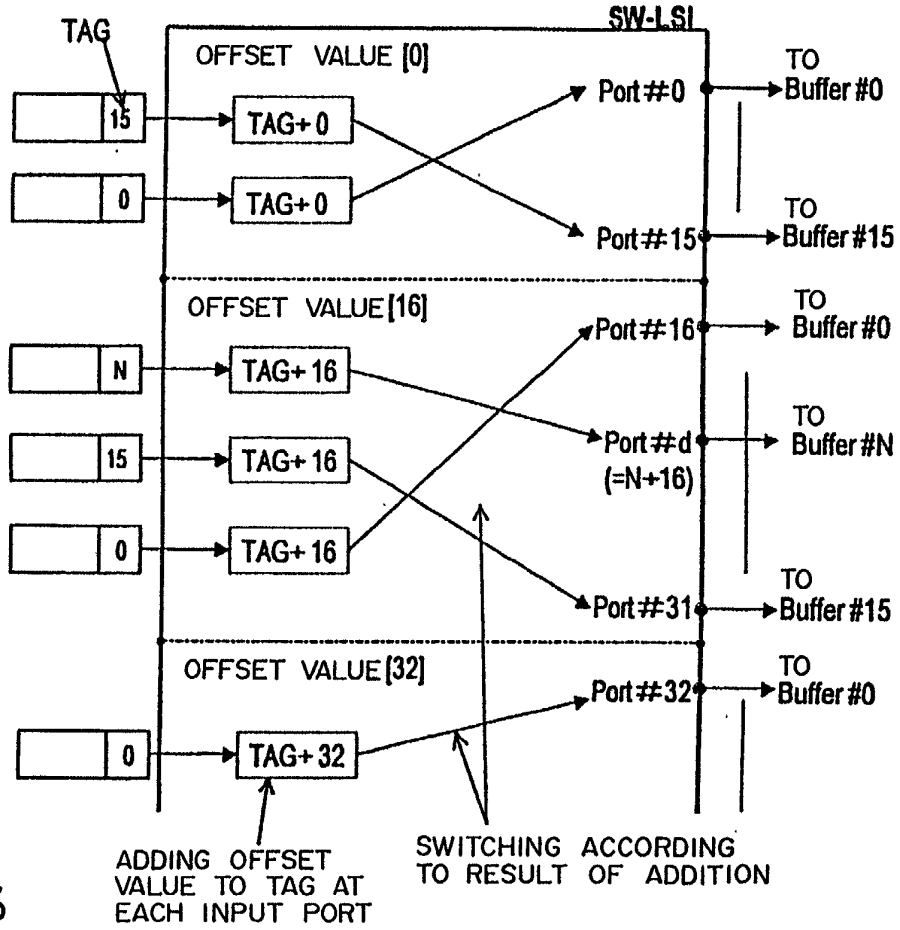


FIG. 33

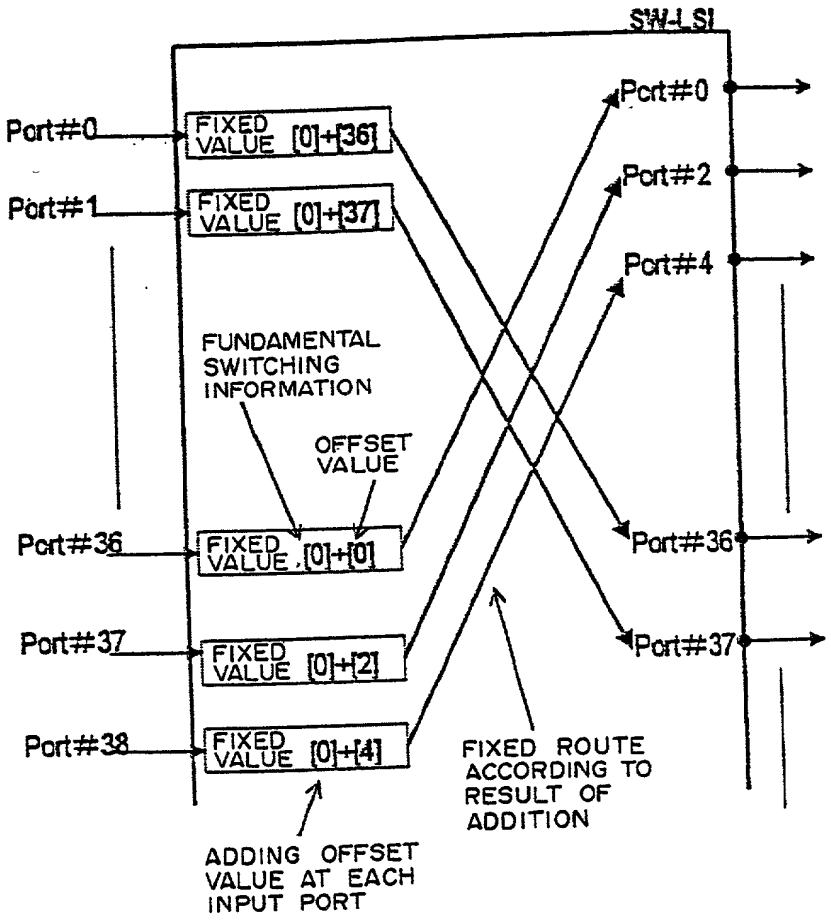

SW-LSI
Port#0
Port#1
Port#36
Port#37
Port#38
FIXED VALUE [0]+[36]
FIXED VALUE [0]+[37]
FIXED VALUE [0]+[0]
FIXED VALUE [0]+[2]
FIXED VALUE [0]+[4]
FUNDAMENTAL SWITCHING INFORMATION
OFFSET VALUE
ADDING OFFSET VALUE AT EACH INPUT PORT
FIXED ROUTE ACCORDING TO RESULT OF ADDITION
Port#0
Port#2
Port#4
Port#36
Port#37

FIG. 34

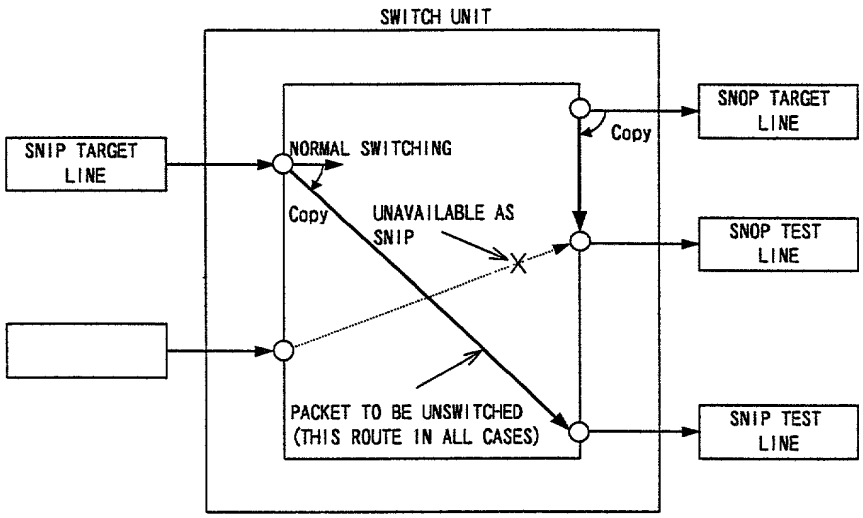

SWITCH UNIT
SNIP TARGET LINE
NORMAL SWITCHING
Copy
UNAVAILABLE AS SNIP
PACKET TO BE UNSWITCHED (THIS ROUTE IN ALL CASES)
Copy
SNOP TARGET LINE
SNOP TEST LINE
SNIP TEST LINE

FIG. 35

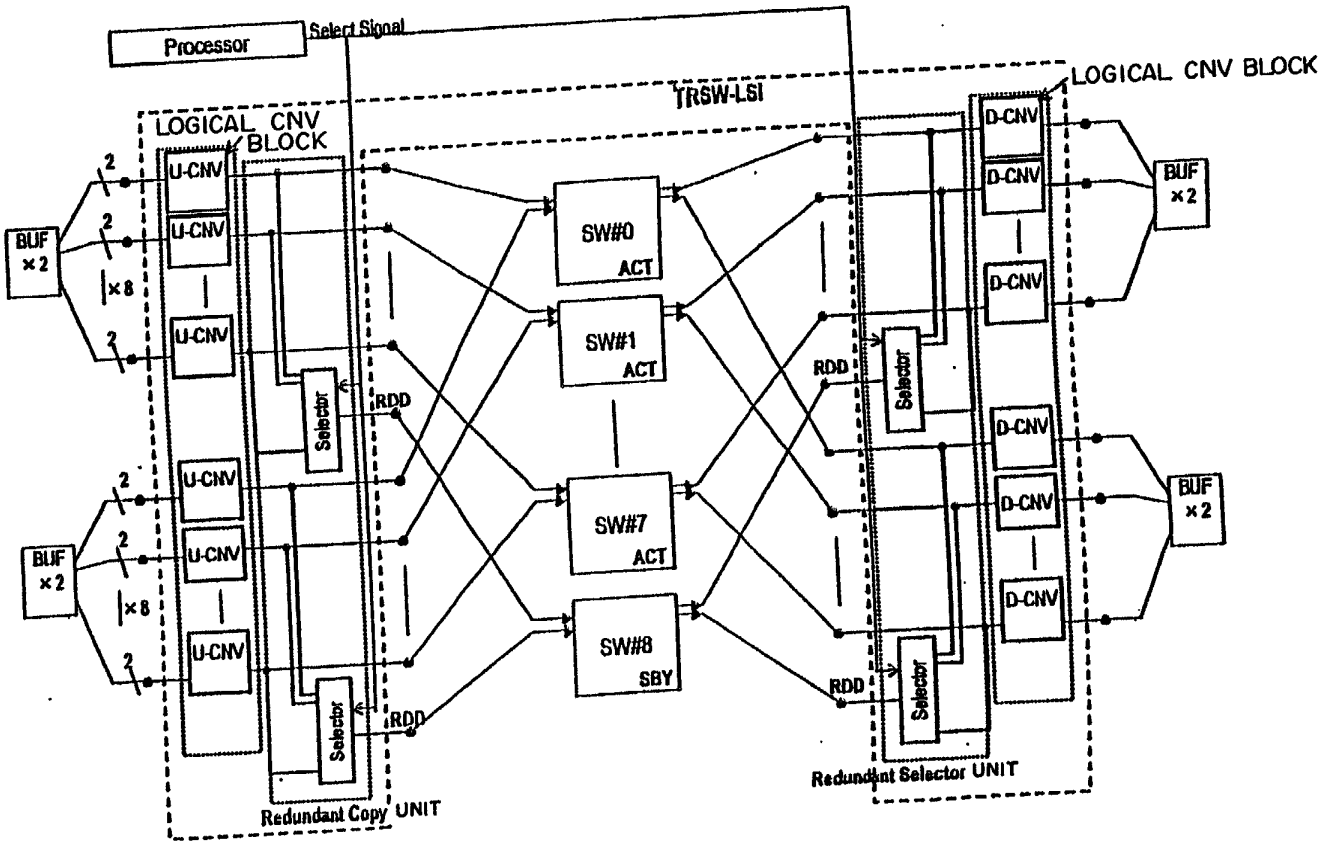

Processor
Select Signal
TRSW-LSI
LOGICAL CNV BLOCK
LOGICAL CNV BLOCK
BUF ×2
BUF ×2
BUF ×2
BUF ×2
×8
×8
2
U-CNV
U-CNV
U-CNV
U-CNV
U-CNV
U-CNV
Selector
Selector
RDD
RDD
SW#0 ACT
SW#1 ACT
SW#7 ACT
SW#8 SBY
D-CNV
D-CNV
D-CNV
D-CNV
D-CNV
D-CNV
Selector
Selector
RDD
RDD
Redundant Copy UNIT
Redundant Selector UNIT

FIG. 36

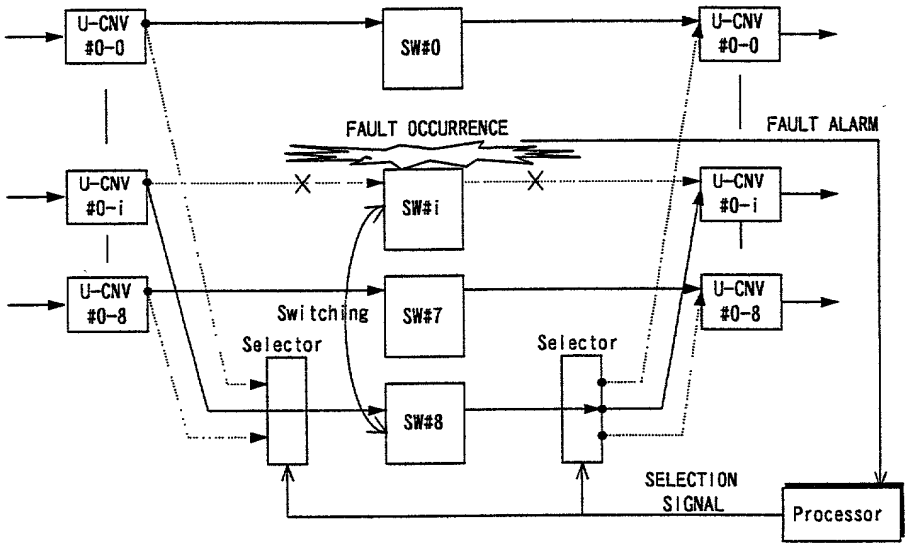

U-CNV
#0-0
SW#0
U-CNV
#0-0
FAULT OCCURRENCE
FAULT ALARM
U-CNV
#0-i
SW#i
U-CNV
#0-i
U-CNV
#0-8
Switching
SW#7
U-CNV
#0-8
Selector
Selector
SW#8
SELECTION
SIGNAL
Processor

FIG. 37

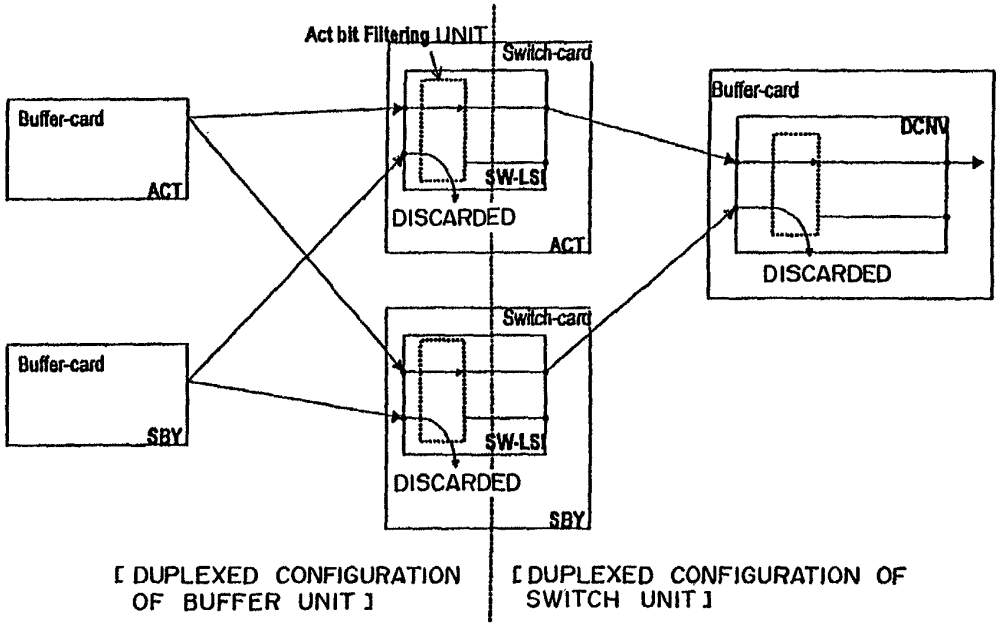


FIG. 38

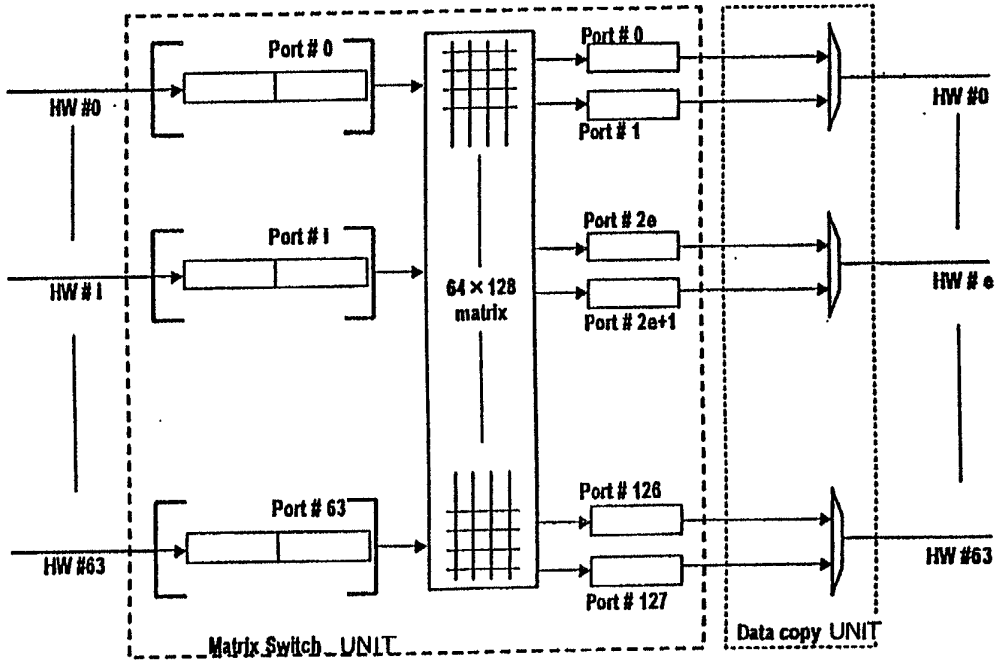


FIG. 39

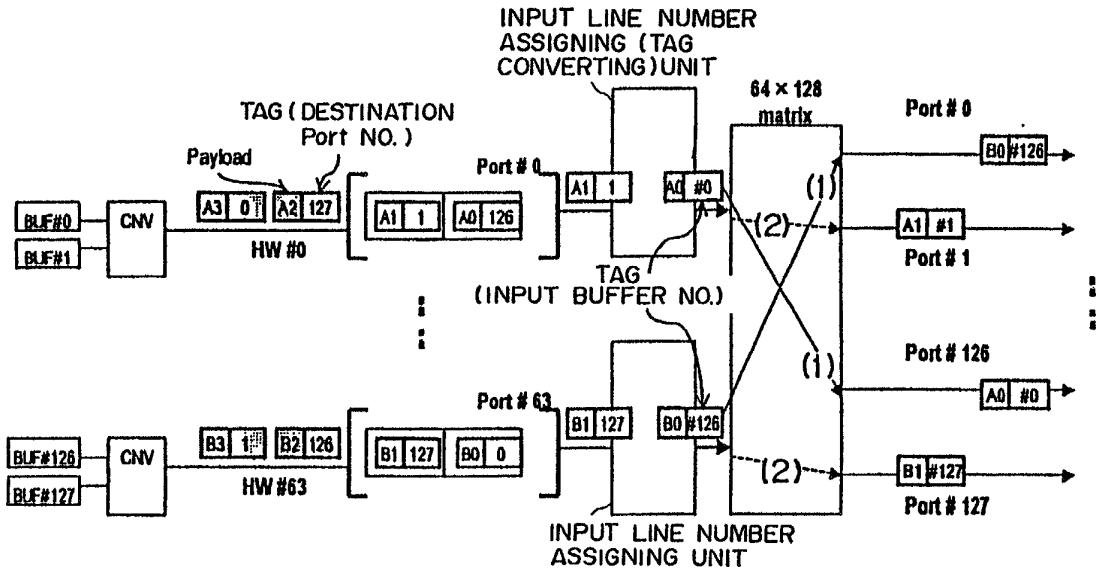

INPUT LINE NUMBER ASSIGNING (TAG CONVERTING) UNIT
64 × 128 matrix
TAG (DESTINATION Port NO.)
Payload
Port # 0
BUF#0
BUF#1
CNV
HW #0
A3 0
A2 127
A1 1
A0 126
A1 1
A0 #0
TAG (INPUT BUFFER NO.)
(1)
(2)
Port # 0
B0 #126
A1 #1
Port # 1
Port # 63
BUF#126
BUF#127
CNV
HW #63
B3 1
B2 126
B1 127
B0 0
B1 127
B0 #126
Port # 126
A0 #0
B1 #127
Port # 127
INPUT LINE NUMBER ASSIGNING UNIT

FIG. 40

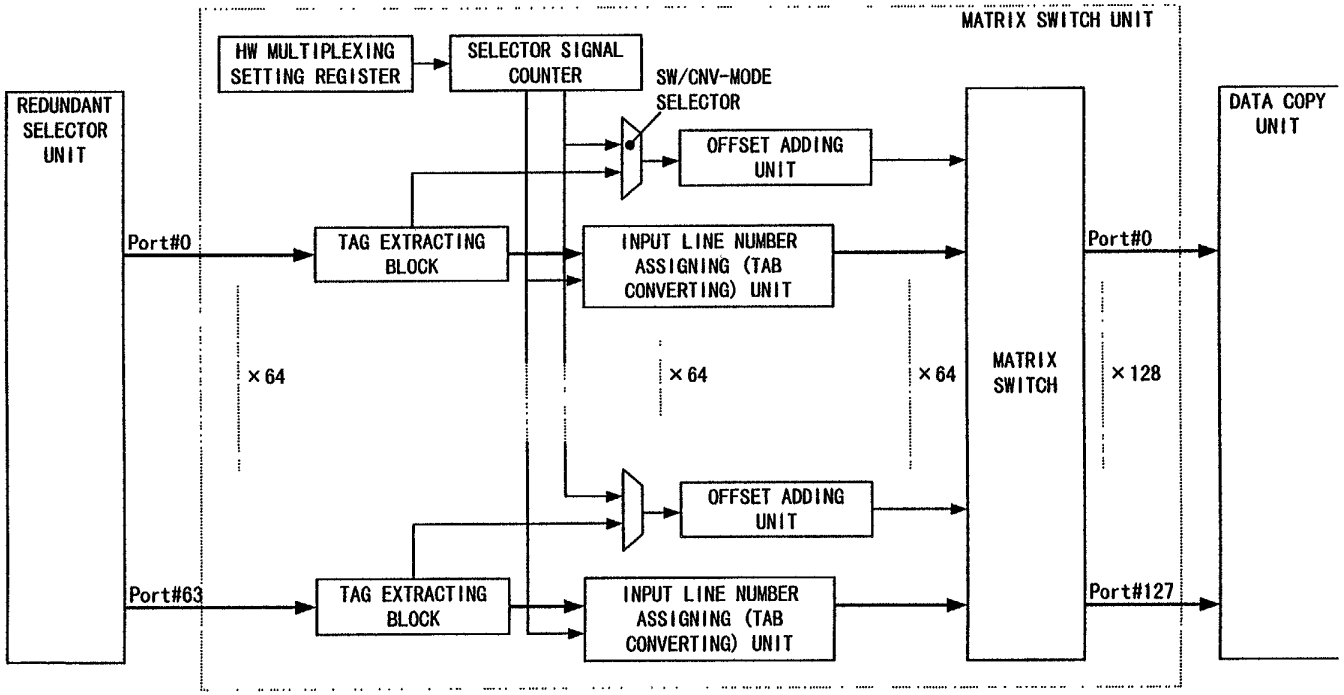

MATRIX SWITCH UNIT
HW MULTIPLEXING SETTING REGISTER
SELECTOR SIGNAL COUNTER
SW/CNV-MODE SELECTOR
REDUNDANT SELECTOR UNIT
OFFSET ADDING UNIT
Port#0
TAG EXTRACTING BLOCK
INPUT LINE NUMBER ASSIGNING (TAB CONVERTING) UNIT
×64
×64
×64
MATRIX SWITCH
×128
Port#0
DATA COPY UNIT
OFFSET ADDING UNIT
Port#63
TAG EXTRACTING BLOCK
INPUT LINE NUMBER ASSIGNING (TAB CONVERTING) UNIT
Port#127

FIG. 41

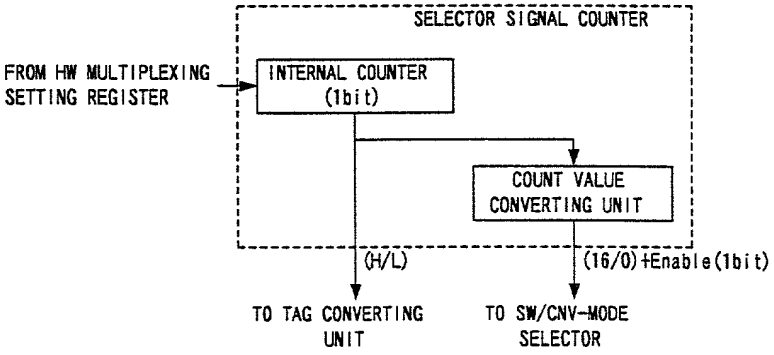

SELECTOR SIGNAL COUNTER
FROM HW MULTIPLEXING SETTING REGISTER
INTERNAL COUNTER (1bit)
COUNT VALUE CONVERTING UNIT
(H/L)
(16/0)+Enable(1bit)
TO TAG CONVERTING UNIT
TO SW/CNV-MODE SELECTOR

FIG. 42

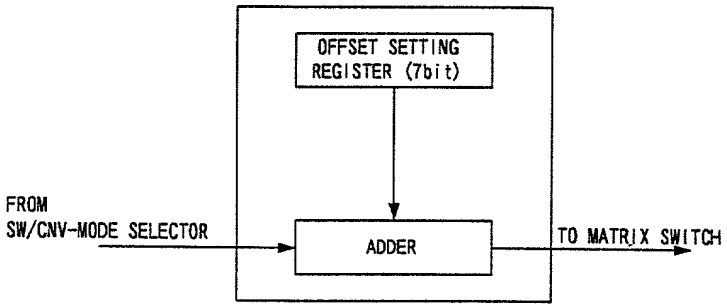

OFFSET SETTING
REGISTER (7bit)
FROM
SW/CNV-MODE SELECTOR
ADDER
TO MATRIX SWITCH

FIG. 43

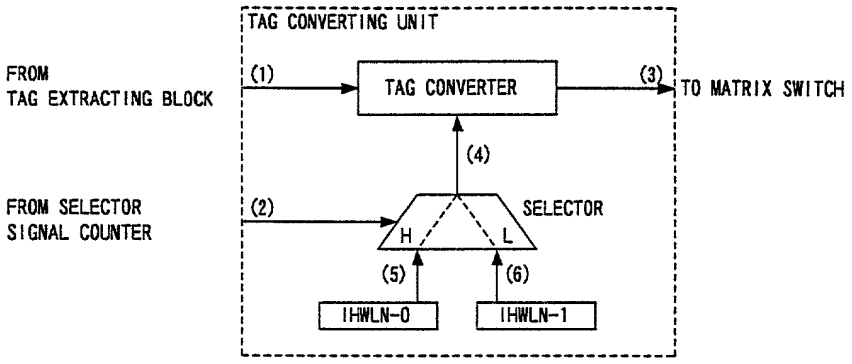

TAG CONVERTING UNIT
FROM
TAG EXTRACTING BLOCK
(1)
TAG CONVERTER
(3)
TO MATRIX SWITCH
(4)
FROM SELECTOR
SIGNAL COUNTER
(2)
SELECTOR
H
L
(5)
(6)
IHWLN-0
IHWLN-1

FIG. 44

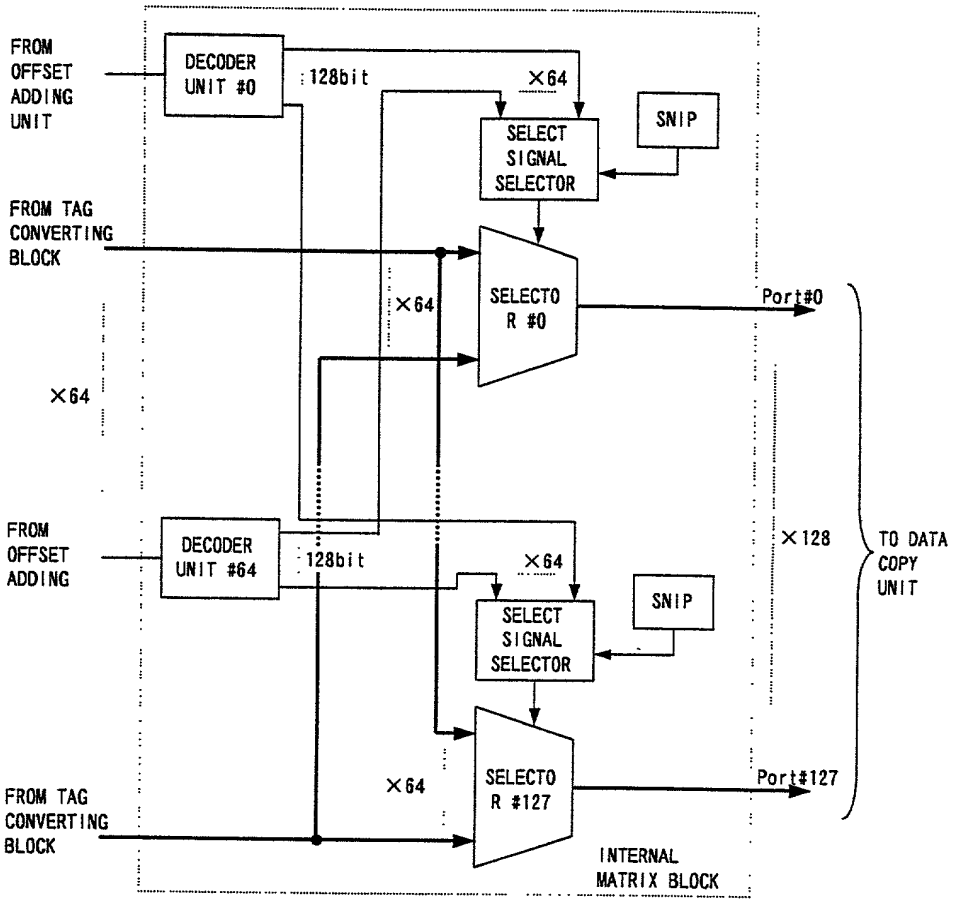

FROM OFFSET ADDING UNIT
DECODER UNIT #0
128bit
×64
SELECT SIGNAL SELECTOR
SNIP
FROM TAG CONVERTING BLOCK
×64
SELECTO R #0
Port#0
×64
FROM OFFSET ADDING
DECODER UNIT #64
128bit
×64
SELECT SIGNAL SELECTOR
SNIP
×128
TO DATA COPY UNIT
×64
SELECTO R #127
Port#127
FROM TAG CONVERTING BLOCK
INTERNAL MATRIX BLOCK

FIG. 45

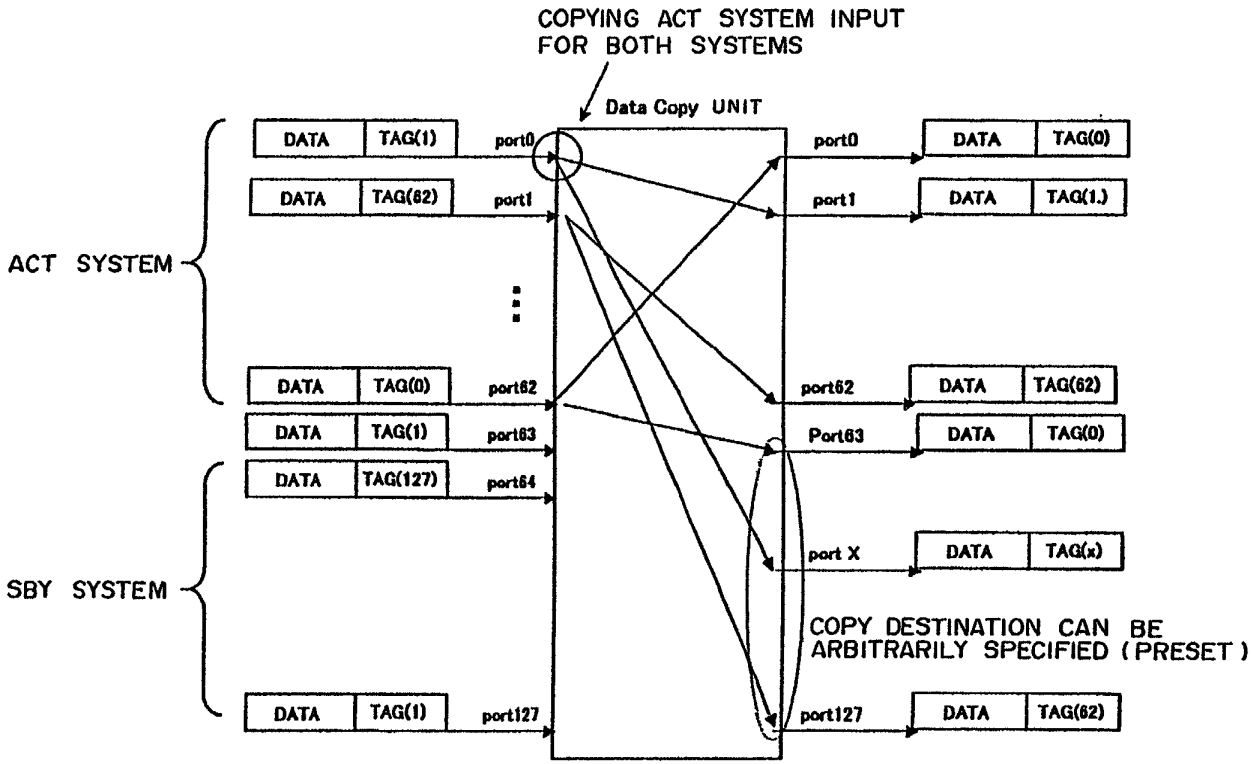


FIG. 46

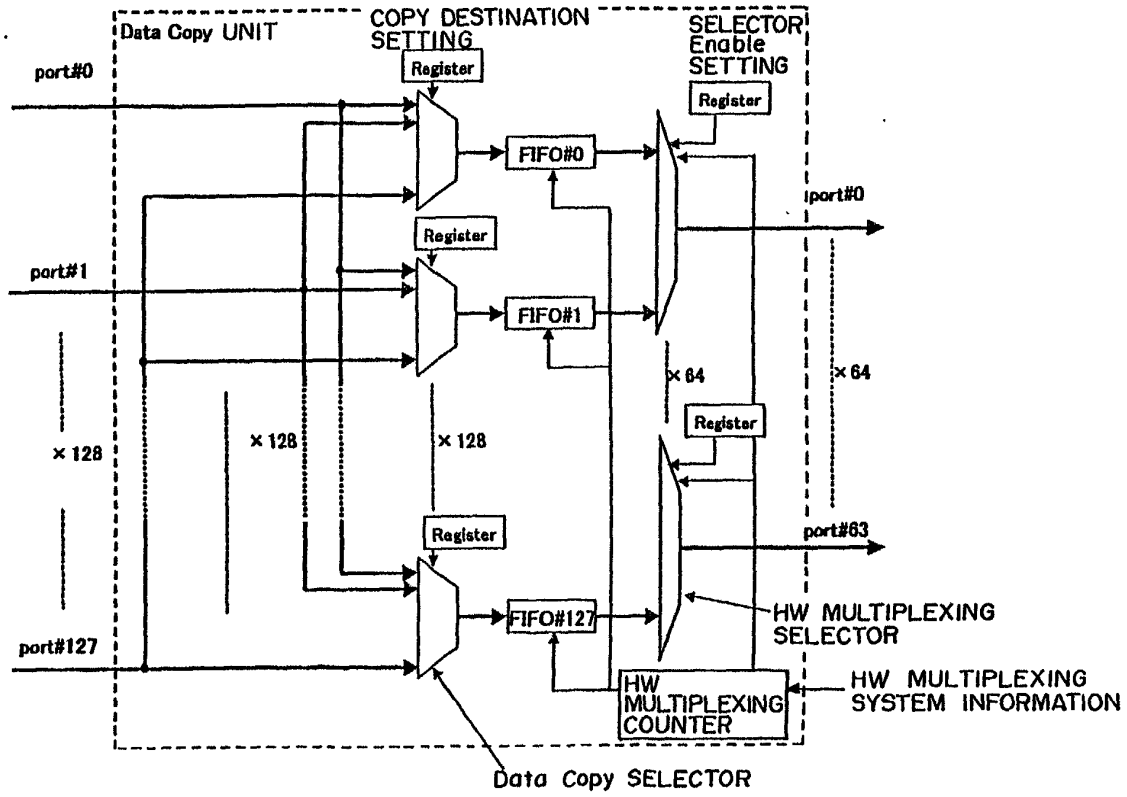

Data Copy UNIT
COPY DESTINATION SETTING
SELECTOR Enable SETTING
port#0
Register
FIFO#0
Register
port#0
port#1
Register
FIFO#1
× 64
× 64
× 128
× 128
× 128
Register
Register
port#63
FIFO#127
HW MULTIPLEXING SELECTOR
port#127
HW MULTIPLEXING COUNTER
HW MULTIPLEXING SYSTEM INFORMATION
Data Copy SELECTOR

FIG. 47

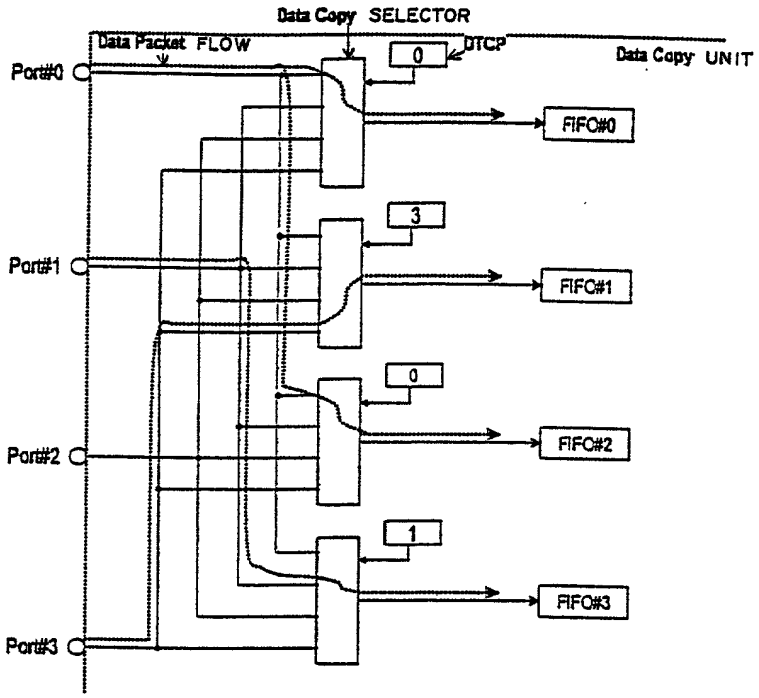

Data Copy SELECTOR
Data Packet FLOW
DTCP
Data Copy UNIT
Port#0
Port#1
Port#2
Port#3
0
3
0
1
FIFO#0
FIFO#1
FIFO#2
FIFO#3

FIG. 48

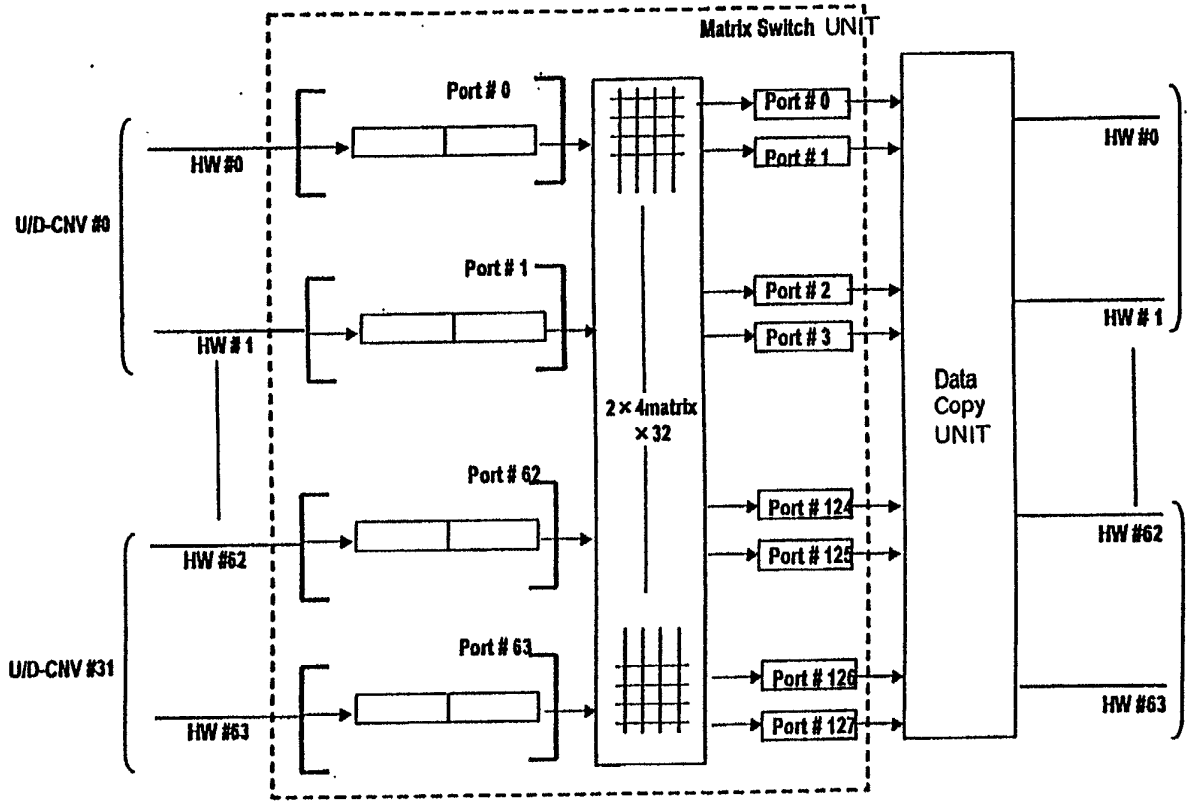

Matrix Switch UNIT
Port # 0
Port # 1
Port # 62
Port # 63
HW #0
HW # 1
HW #62
HW #63
U/D-CNV #0
U/D-CNV #31
2 × 4matrix
× 32
Port # 0
Port # 1
Port # 2
Port # 3
Port # 124
Port # 125
Port # 126
Port # 127
Data
Copy
UNIT
HW #0
HW # 1
HW #62
HW #63

FIG. 49

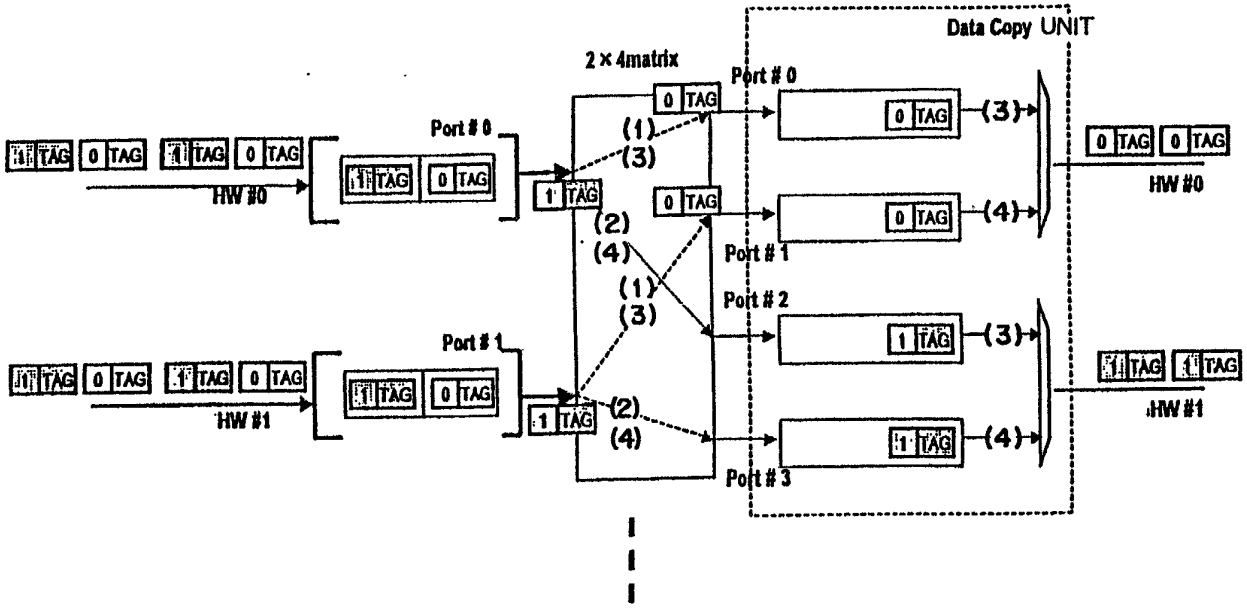

Data Copy UNIT
2 × 4matrix
Port # 0
Port # 1
Port # 2
Port # 3
HW #0
HW #1
TAG
(1)
(2)
(3)
(4)

FIG. 50

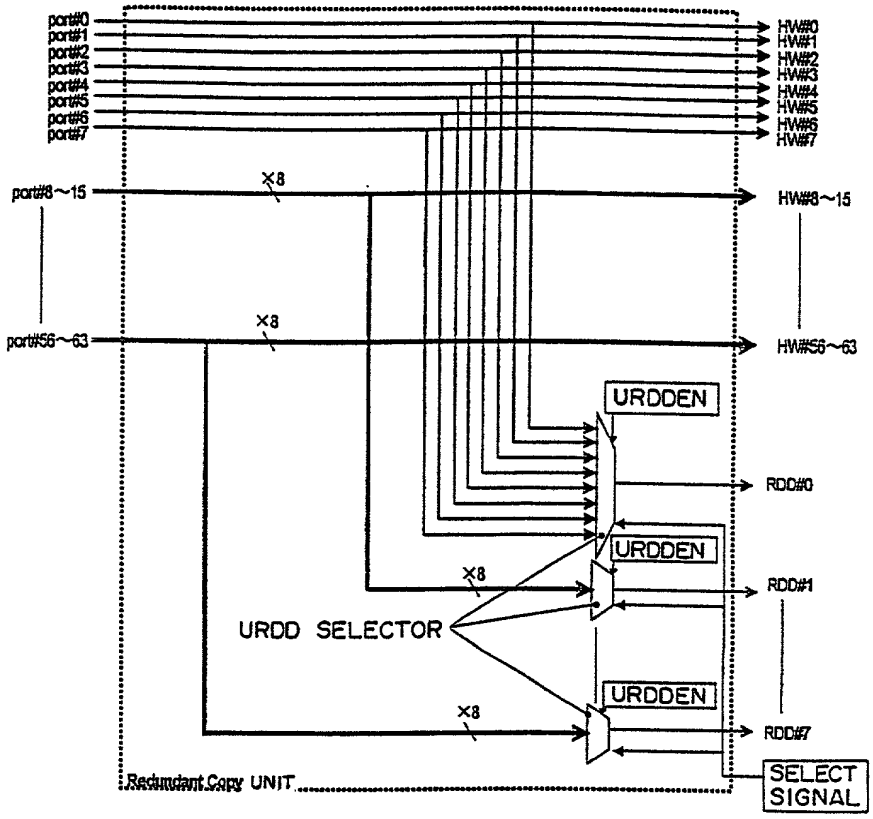

port#0
port#1
port#2
port#3
port#4
port#5
port#6
port#7
HW#0
HW#1
HW#2
HW#3
HW#4
HW#5
HW#6
HW#7
port#8~15
×8
HW#8~15
port#56~63
×8
HW#56~63
URDDEN
RDD#0
URDDEN
×8
RDD#1
URDD SELECTOR
URDDEN
×8
RDD#7
Redundant Copy UNIT
SELECT SIGNAL

FIG. 51

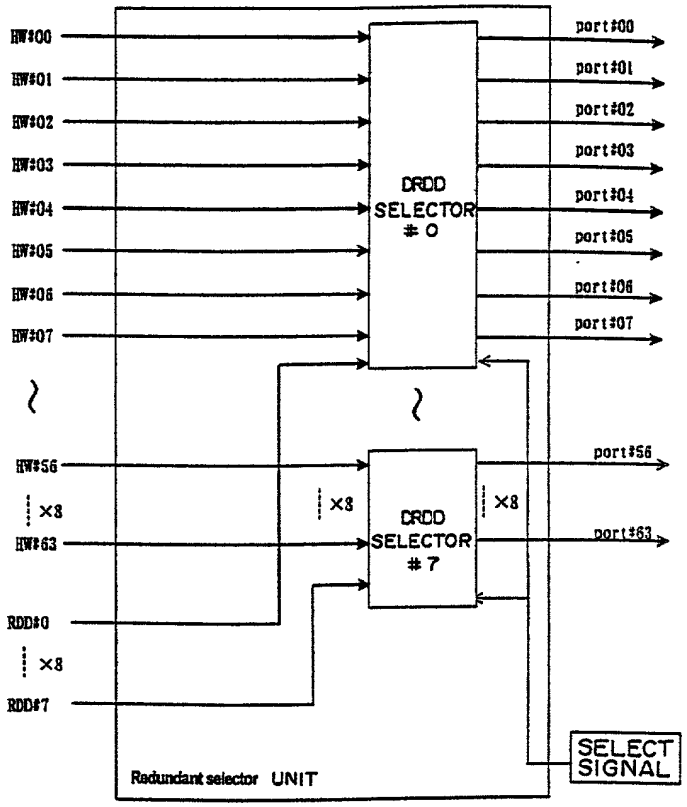

HW#00
HW#01
HW#02
HW#03
HW#04
HW#05
HW#06
HW#07
HW#56
×8
HW#63
RDD#0
×8
RDD#7
DRDD SELECTOR # 0
DRDD SELECTOR # 7
×8
×8
port#00
port#01
port#02
port#03
port#04
port#05
port#06
port#07
port#56
port#63
SELECT SIGNAL
Redundant selector UNIT

FIG. 52

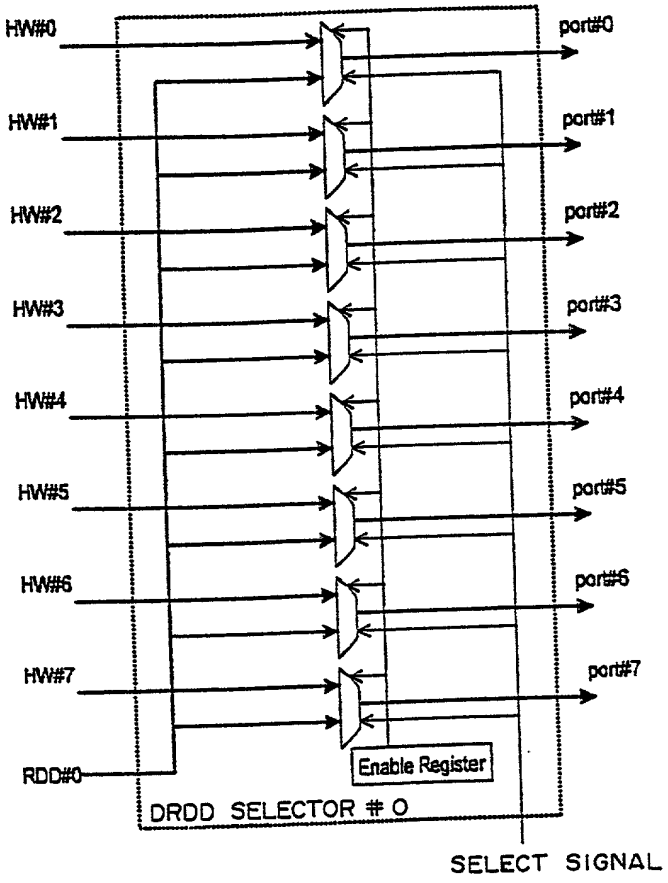

HW#0
HW#1
HW#2
HW#3
HW#4
HW#5
HW#6
HW#7
RDD#0
port#0
port#1
port#2
port#3
port#4
port#5
port#6
port#7
Enable Register
DRDD SELECTOR # 0
SELECT SIGNAL

FIG. 53

TABLE 1 SW-CARD CONFIGURATION BY SWITCH CAPACITY

MAXIMUM SWITCH CAPACITY (bps)	NUMBER OF SWITCH CARDS (EXCLUDING REDUNDANT SYSTEM)	
2.56T	8	
1.28T	4	
640G	2	
320G	1	

FIG. 54A

TABLE 2 BUFFER CARD TYPE

Buffer-Card CAPACITY (bps)	NUMBER OF ACCOMMODATED LINES	NUMBER OF TRSW-LSIs (DNV-mode)
160G	8	2
80G	4	2
40G	2	1
20G	1	1

FIG. 54B

TABLE 3 SW-CARD CONFIGURATION AND BUFFER CARD ALLOWED

SW-CARD CONFIGURATION (NUMBER OF CARDS)	BUFFER CARD ALLOWED	
8	160G, 80G, 40G, 20G	
4	80G, 40G, 20G	
2	40G, 20G	
1	20G	

FIG. 54C

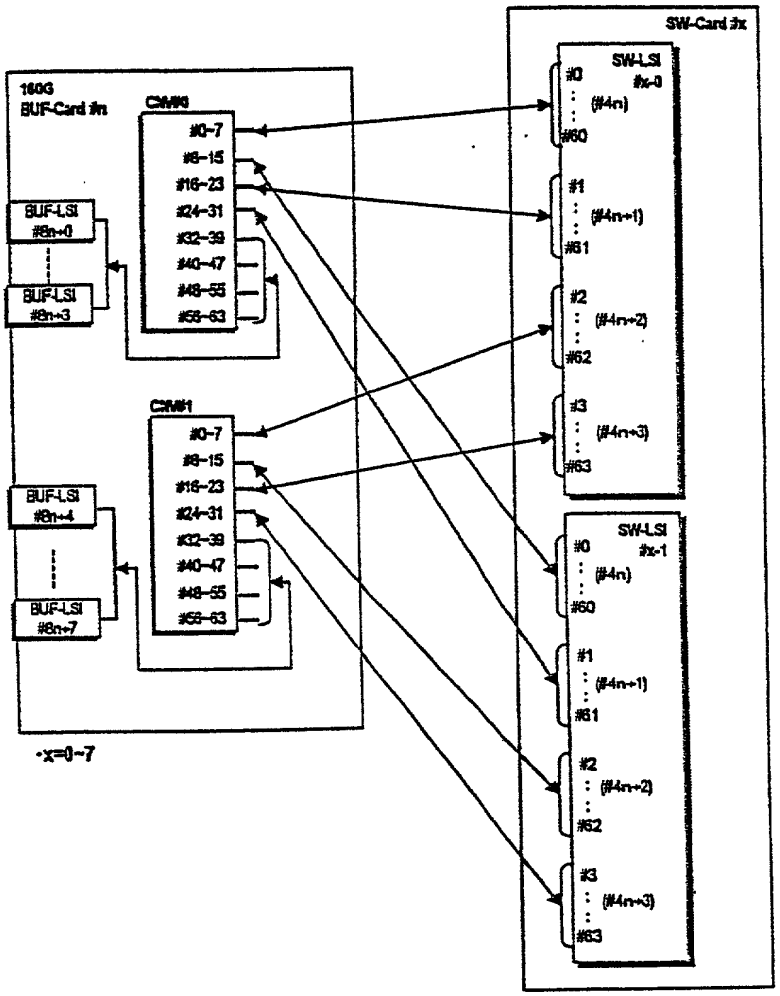

160G
BUF-Card #n
CM#0
#0-7
#8-15
#16-23
#24-31
#32-39
#40-47
#48-55
#56-63
BUF-LSI
#8n+0
BUF-LSI
#8n+3
CM#1
#0-7
#8-15
#16-23
#24-31
#32-39
#40-47
#48-55
#56-63
BUF-LSI
#8n+4
BUF-LSI
#8n+7
·x=0~7
SW-Card #x
SW-LSI
#x-0
#0
(#4n)
#60
#1
(#4n+1)
#61
#2
(#4n+2)
#62
#3
(#4n+3)
#63
SW-LSI
#x-1
#0
(#4n)
#60
#1
(#4n+1)
#61
#2
(#4n+2)
#62
#3
(#4n+3)
#63

FIG. 55

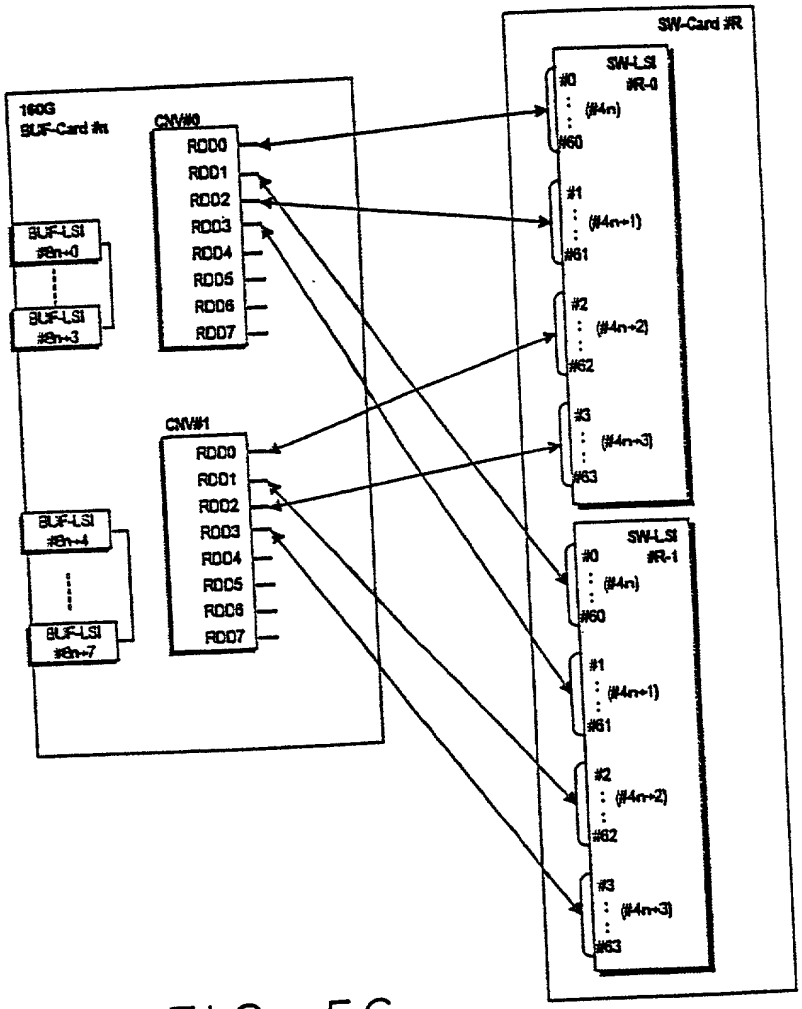

160G
BUF-Card #n
CNV#0
RDD0
RDD1
RDD2
RDD3
RDD4
RDD5
RDD6
RDD7
BUF-LSI
#8n+0
BUF-LSI
#8n+3
CNV#1
RDD0
RDD1
RDD2
RDD3
RDD4
RDD5
RDD6
RDD7
BUF-LSI
#8n+4
BUF-LSI
#8n+7
SW-Card #R
SW-LSI
#R-0
#0
(#4n)
#60
#1
(#4n+1)
#61
#2
(#4n+2)
#62
#3
(#4n+3)
#63
SW-LSI
#R-1
#0
(#4n)
#60
#1
(#4n+1)
#61
#2
(#4n+2)
#62
#3
(#4n+3)
#63

FIG. 56

TABLE 4 CNV EXTERNAL TERMINAL CONNECTION CONFIGURATION

EXTERNAL TERMINAL No. (DAT#)	CONNECTION DESTINATION		
	Card (TYPE, No.)	LSI No.	EXTERNAL TERMINAL No.
00	SW#0	0	4n[4n+2]
01	SW#1	0	4n[4n+2]
02	SW#2	0	4n[4n+2]
03	SW#3	0	4n[4n+2]
04	SW#4	0	4n[4n+2]
05	SW#5	0	4n[4n+2]
06	SW#6	0	4n[4n+2]
07	SW#7	0	4n[4n+2]
08	SW#0	1	4n[4n+2]
09	SW#1	1	4n[4n+2]
10	SW#2	1	4n[4n+2]
11	SW#3	1	4n[4n+2]
12	SW#4	1	4n[4n+2]

FIG. 57

EXTERNAL TERMINAL No. (DAT#)	CONNECTION DESTINATION		
	Card (TYPE, No.)	LSI No.	EXTERNAL TERMINAL No.
13	SW#5	1	4n[4n+2]
14	SW#6	1	4n[4n+2]
15	SW#7	1	4n[4n+2]
16	SW#0	0	4n+1[4n+3]
17	SW#1	0	4n+1[4n+3]
18	SW#2	0	4n+1[4n+3]
19	SW#3	0	4n+1[4n+3]
20	SW#4	0	4n+1[4n+3]
21	SW#5	0	4n+1[4n+3]
22	SW#6	0	4n+1[4n+3]
23	SW#7	0	4n+1[4n+3]
24	SW#0	1	4n+1[4n+3]
25	SW#1	1	4n+1[4n+3]
26	SW#2	1	4n+1[4n+3]
27	SW#3	1	4n+1[4n+3]
28	SW#4	1	4n+1[4n+3]
29	SW#5	1	4n+1[4n+3]
30	SW#6	1	4n+1[4n+3]
31	SW#7	1	4n+1[4n+3]
32	BUF#n	8n[8n+4]	0
33	BUF#n	8n[8n+4]	1
34	BUF#n	8n[8n+4]	2
35	BUF#n	8n[8n+4]	3
36	BUF#n	8n[8n+4]	4
37	BUF#n	8n[8n+4]	5
38	BUF#n	8n[8n+4]	6
39	BUF#n	8n[8n+4]	7
40	BUF#n	8n+1[8n+5]	0
41	BUF#n	8n+1[8n+5]	1
42	BUF#n	8n+1[8n+5]	2
43	BUF#n	8n+1[8n+5]	3
44	BUF#n	8n+1[8n+5]	4
45	BUF#n	8n+1[8n+5]	5
46	BUF#n	8n+1[8n+5]	6
47	BUF#n	8n+1[8n+5]	7
48	BUF#n	8n+2[8n+6]	0
49	BUF#n	8n+2[8n+6]	1
50	BUF#n	8n+2[8n+6]	2
51	BUF#n	8n+2[8n+6]	3
52	BUF#n	8n+2[8n+6]	4
53	BUF#n	8n+2[8n+6]	5
54	BUF#n	8n+2[8n+6]	6
55	BUF#n	8n+2[8n+6]	7
56	BUF#n	8n+3[8n+7]	0
57	BUF#n	8n+3[8n+7]	1
58	BUF#n	8n+3[8n+7]	2

FIG. 58

EXTERNAL TERMINAL No. (DAT#)	CONNECTION DESTINATION		
	Card (TYPE, No.)	LSI No.	EXTERNAL TERMINAL No.
59	BUF#n	8n+3[8n+7]	3
60	BUF#n	8n+3[8n+7]	4
61	BUF#n	8n+3[8n+7]	5
62	BUF#n	8n+3[8n+7]	6
63	BUF#n	8n+3[8n+7]	7
RDD 0	SW#R	0	4n[4n+2]
RDD 1	SW#R	1	4n[4n+2]
RDD 2	SW#R	0	4n+1[4n+3]
RDD 3	SW#R	1	4n+1[4n+3]
RDD 4	—	—	—
RDD 5	—	—	—
RDD 6	—	—	—
RDD 7	—	—	—

(*) n; BUFFER CARD No. (0～7)
-; UNCONNECTED

FIG. 59

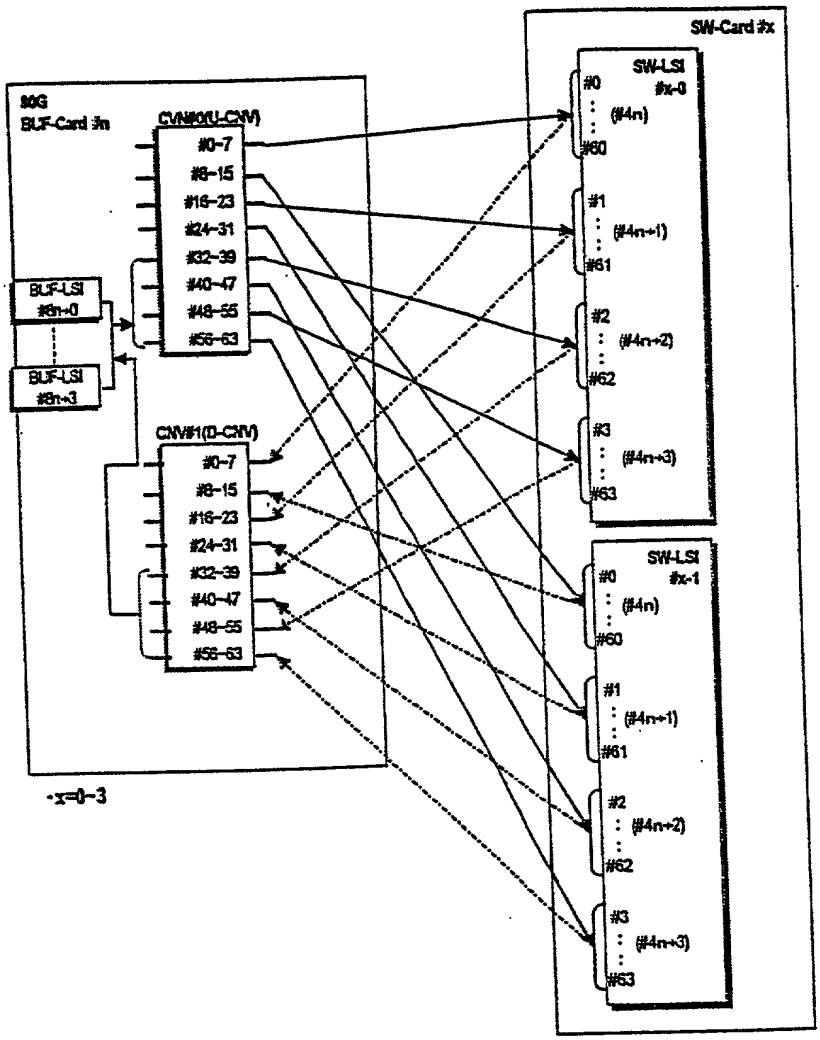

SW-Card #x
80G
BUF-Card #n
CVN#0(U-CNV)
#0-7
#8-15
#16-23
#24-31
#32-39
#40-47
#48-55
#56-63
BUF-LSI
#8n+0
BUF-LSI
#8n+3
CVN#1(D-CNV)
#0-7
#8-15
#16-23
#24-31
#32-39
#40-47
#48-55
#56-63
x=0-3
SW-LSI
#x-0
#0
(#4n)
#60
#1
(#4n+1)
#61
#2
(#4n+2)
#62
#3
(#4n+3)
#63
SW-LSI
#x-1
#0
(#4n)
#60
#1
(#4n+1)
#61
#2
(#4n+2)
#62
#3
(#4n+3)
#63

FIG. 60

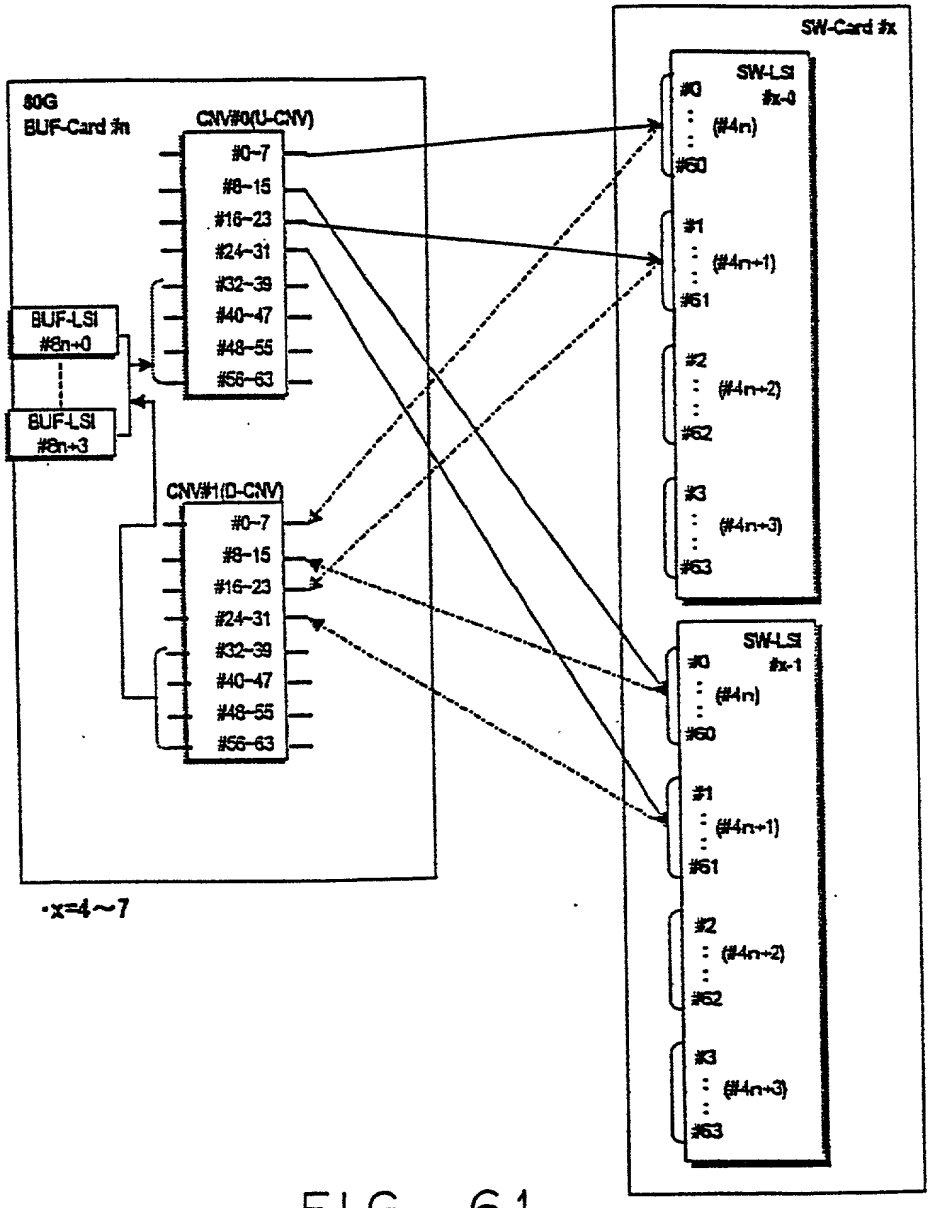

SW-Card #x
80G
BUF-Card #n
CNV#0(U-CNV)
#0-7
#8-15
#16-23
#24-31
#32-39
#40-47
#48-55
#56-63
BUF-LSI
#8n+0
BUF-LSI
#8n+3
CNV#1(D-CNV)
#0-7
#8-15
#16-23
#24-31
#32-39
#40-47
#48-55
#56-63
SW-LSI
#x-0
#0
(#4n)
#60
#1
(#4n+1)
#61
#2
(#4n+2)
#62
#3
(#4n+3)
#63
SW-LSI
#x-1
#0
(#4n)
#60
#1
(#4n+1)
#61
#2
(#4n+2)
#62
#3
(#4n+3)
#63
・x=4～7

FIG. 61

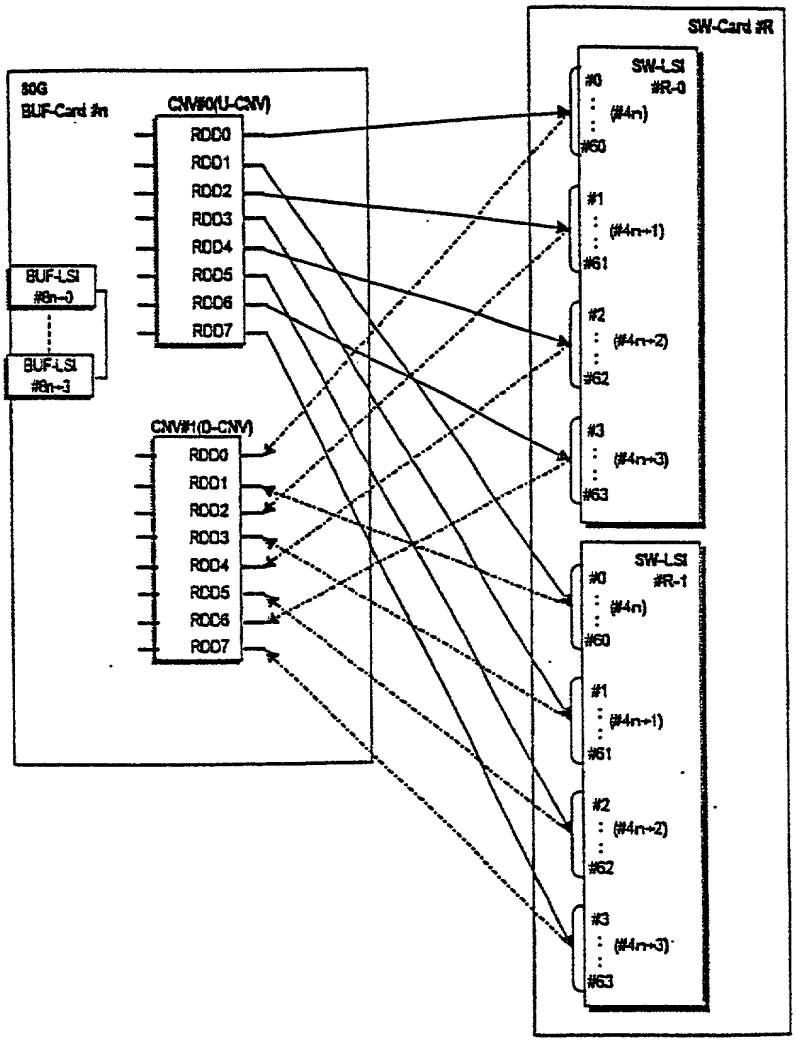

SW-Card #R
SOG
BUF-Card #n
CNV#0(U-CNV)
RDD0
RDD1
RDD2
RDD3
RDD4
RDD5
RDD6
RDD7
BUF-LSI
#8n-0
BUF-LSI
#8n-3
CNV#1(D-CNV)
RDD0
RDD1
RDD2
RDD3
RDD4
RDD5
RDD6
RDD7
SW-LSI
#R-0
#0
(#4n)
#60
#1
(#4n+1)
#61
#2
(#4n+2)
#62
#3
(#4n+3)
#63
SW-LSI
#R-1
#0
(#4n)
#60
#1
(#4n+1)
#61
#2
(#4n+2)
#62
#3
(#4n+3)
#63

FIG. 62

TABLE 5 CNV EXTERNAL TERMINAL CONNECTION CONFIGURATION
(CNV#0 INPUT AND CNV#1 OUTPUT)

EXTERNAL TERMINAL No. (DAT#)	CONNECTION DESTINATION		
	Card (TYPE, No.)	LSI No.	EXTERNAL TERMINAL No.
00	—	—	—
01	—	—	—
02	—	—	—
03	—	—	—
04	—	—	—
05	—	—	—
06	—	—	—
07	—	—	—
08	—	—	—

FIG. 63

EXTERNAL TERMINAL No. (DAT#)	CONNECTION DESTINATION		
	Card (TYPE, No.)	LSI No.	EXTERNAL TERMINAL No.
09	—	—	—
10	—	—	—
11	—	—	—
12	—	—	—
13	—	—	—
14	—	—	—
15	—	—	—
16	—	—	—
17	—	—	—
18	—	—	—
19	—	—	—
20	—	—	—
21	—	—	—
22	—	—	—
23	—	—	—
24	—	—	—
25	—	—	—
26	—	—	—
27	—	—	—
28	—	—	—
29	—	—	—
30	—	—	—
31	—	—	—
32	BUF#n	8n	0
33	BUF#n	8n	1
34	BUF#n	8n	2
35	BUF#n	8n	3
36	BUF#n	8n	4
37	BUF#n	8n	5
38	BUF#n	8n	6
39	BUF#n	8n	7
40	BUF#n	8n+1	0
41	BUF#n	8n+1	1
42	BUF#n	8n+1	2
43	BUF#n	8n+1	3
44	BUF#n	8n+1	4
45	BUF#n	8n+1	5
46	BUF#n	8n+1	6
47	BUF#n	8n+1	7
48	BUF#n	8n+2	0
49	BUF#n	8n+2	1
50	BUF#n	8n+2	2
51	BUF#n	8n+2	3
52	BUF#n	8n+2	4
53	BUF#n	8n+2	5
54	BUF#n	8n+2	6

FIG. 64

EXTERNAL TERMINAL No. (DAT#)	CONNECTION DESTINATION		
	Card (TYPE, No.)	LSI No.	EXTERNAL TERMINAL No.
55	BUF#n	8n+2	7
56	BUF#n	8n+3	0
57	BUF#n	8n+3	1
58	BUF#n	8n+3	2
59	BUF#n	8n+3	3
60	BUF#n	8n+3	4
61	BUF#n	8n+3	5
62	BUF#n	8n+3	6
63	BUF#n	8n+3	7
RDD 0	—	—	—
RDD 1	—	—	—
RDD 2	—	—	—
RDD 3	—	—	—
RDD 4	—	—	—
RDD 5	—	—	—
RDD 6	—	—	—
RDD 7	—	—	—

(*) n; BUFFER CARD No. (0～7)
−; UNCONNECTED

TABLE 6 CNV EXTERNAL TERMINAL CONNECTION CONFIGURATION (CNV#0 OUTPUT AND CNV#1 INPUT)

EXTERNAL TERMINAL No. (DAT#)	CONNECTION DESTINATION		
	Card (TYPE, No.)	LSI No.	EXTERNAL TERMINAL No.
00	SW#0	0	4n
01	SW#1	0	4n
02	SW#2	0	4n
03	SW#3	0	4n
04	SW#4	0	4n
05	SW#5	0	4n
06	SW#6	0	4n
07	SW#7	0	4n
08	SW#0	1	4n
09	SW#1	1	4n
10	SW#2	1	4n
11	SW#3	1	4n
12	SW#4	1	4n
13	SW#5	1	4n
14	SW#6	1	4n
15	SW#7	1	4n
16	SW#0	0	4n+1
17	SW#1	0	4n+1
18	SW#2	0	4n+1
19	SW#3	0	4n+1
20	SW#4	0	4n+1
21	SW#5	0	4n+1

FIG. 65

EXTERNAL TERMINAL No. (DAT#)	CONNECTION DESTINATION		
	Card (TYPE, No.)	LSI No.	EXTERNAL TERMINAL No.
22	SW#6	0	4n+1
23	SW#7	0	4n+1
24	SW#0	1	4n+1
25	SW#1	1	4n+1
26	SW#2	1	4n+1
27	SW#3	1	4n+1
28	SW#4	1	4n+1
29	SW#5	1	4n+1
30	SW#6	1	4n+1
31	SW#7	1	4n+1
32	SW#0	0	4n+2
33	SW#1	0	4n+2
34	SW#2	0	4n+2
35	SW#3	0	4n+2
36	—	—	—
37	—	—	—
38	—	—	—
39	—	—	—
40	SW#0	1	4n+2
41	SW#1	1	4n+2
42	SW#2	1	4n+2
43	SW#3	1	4n+2
44	—	—	—
45	—	—	—
46	—	—	—
47	—	—	—
48	SW#0	0	4n+3
49	SW#1	0	4n+3
50	SW#2	0	4n+3
51	SW#3	0	4n+3
52	—	—	—
53	—	—	—
54	—	—	—
55	—	—	—
56	SW#0	1	4n+3
57	SW#1	1	4n+3
58	SW#2	1	4n+3
59	SW#3	1	4n+3
60	—	—	—
61	—	—	—
62	—	—	—
63	—	—	—
RDD 0	SW#R	0	4n
RDD 1	SW#R	1	4n
RDD 2	SW#R	0	4n+1
RDD 3	SW#R	1	4n+1

FIG. 66

EXTERNAL TERMINAL No. (DAT#)	CONNECTION DESTINATION		
	Card (TYPE, No.)	LSI No.	EXTERNAL TERMINAL No.
RDD 4	SW#R	0	4n+2
RDD 5	SW#R	1	4n+2
RDD 6	SW#R	0	4n+3
RDD 7	SW#R	1	4n+3

(*) n; BUFFER CARD No. (0～7)
-; UNCONNECTED

FIG. 67

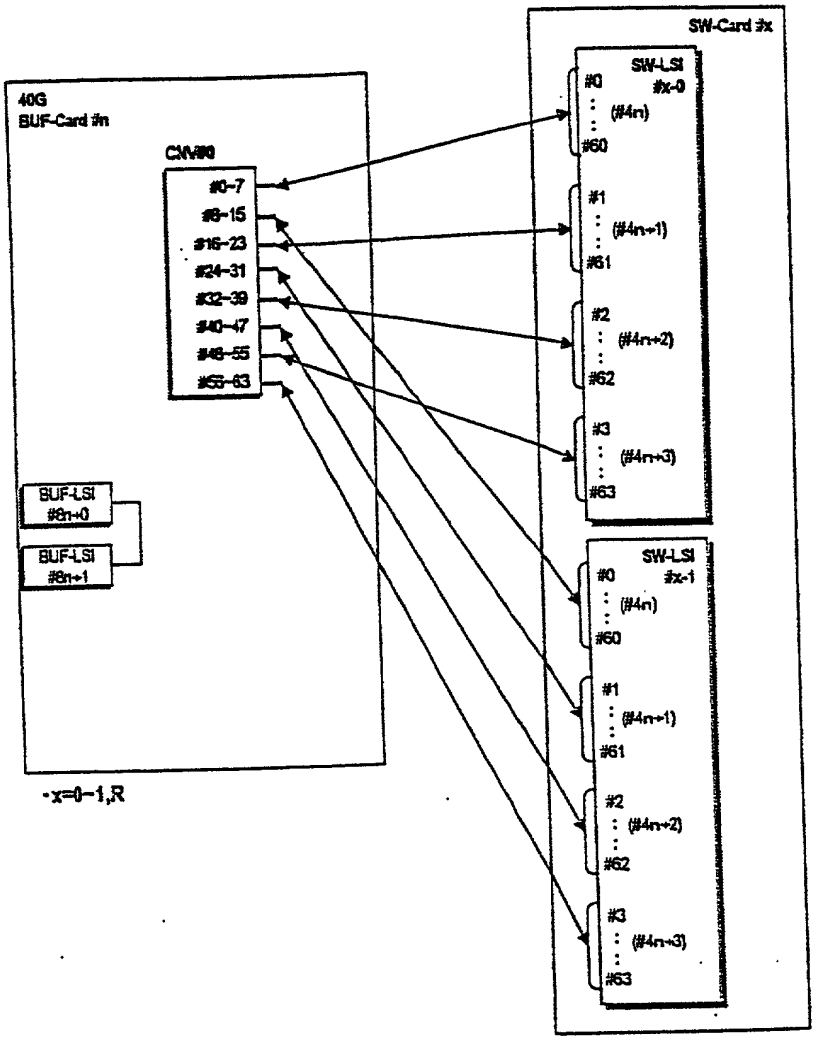

40G
BUF-Card #n
CNW#0
#0-7
#8-15
#16-23
#24-31
#32-39
#40-47
#48-55
#56-63
BUF-LSI
#8n+0
BUF-LSI
#8n+1
-x=0-1,R
SW-Card #x
SW-LSI
#0
#x-0
(#4n)
#60
#1
(#4n+1)
#61
#2
(#4n+2)
#62
#3
(#4n+3)
#63
SW-LSI
#0
#x-1
(#4n)
#60
#1
(#4n+1)
#61
#2
(#4n+2)
#62
#3
(#4n+3)
#63

FIG. 68

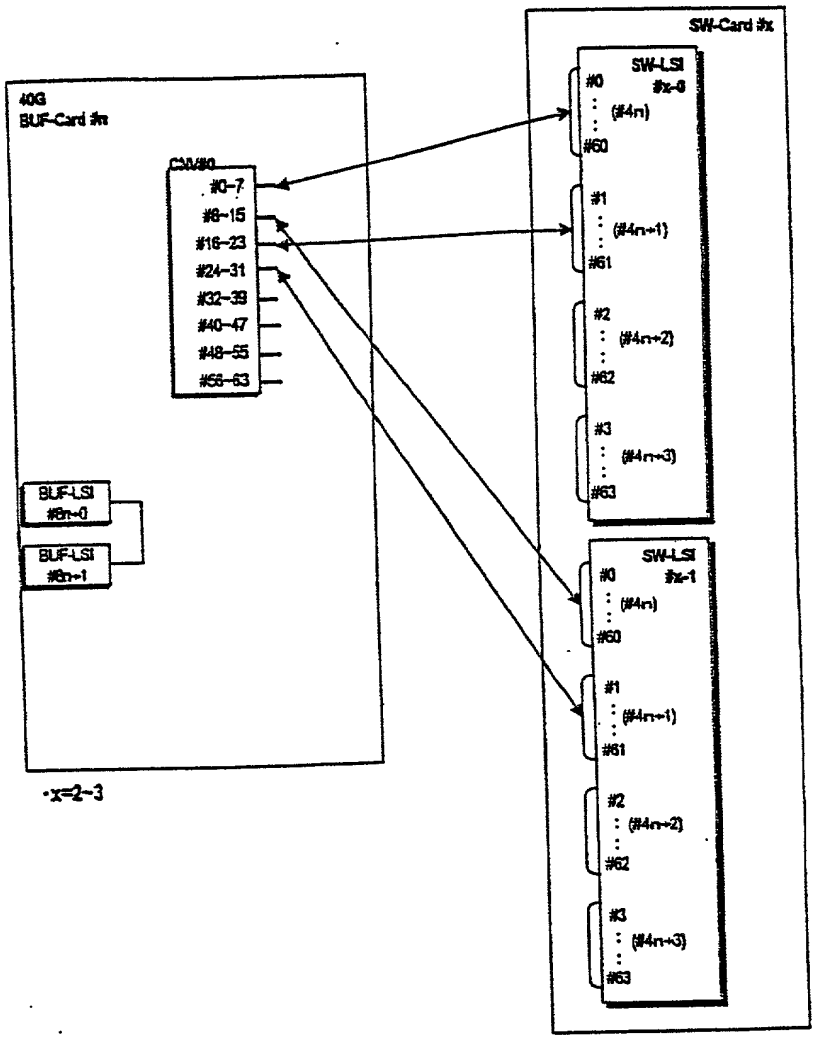

40G
BUF-Card #n
CON#0
#0-7
#8-15
#16-23
#24-31
#32-39
#40-47
#48-55
#56-63
BUF-LSI
#8n+0
BUF-LSI
#8n+1
x=2~3
SW-Card #x
SW-LSI
#0
#x-0
(#4n)
#60
#1
(#4n+1)
#61
#2
(#4n+2)
#62
#3
(#4n+3)
#63
SW-LSI
#0
#x-1
(#4n)
#60
#1
(#4n+1)
#61
#2
(#4n+2)
#62
#3
(#4n+3)
#63

FIG. 69

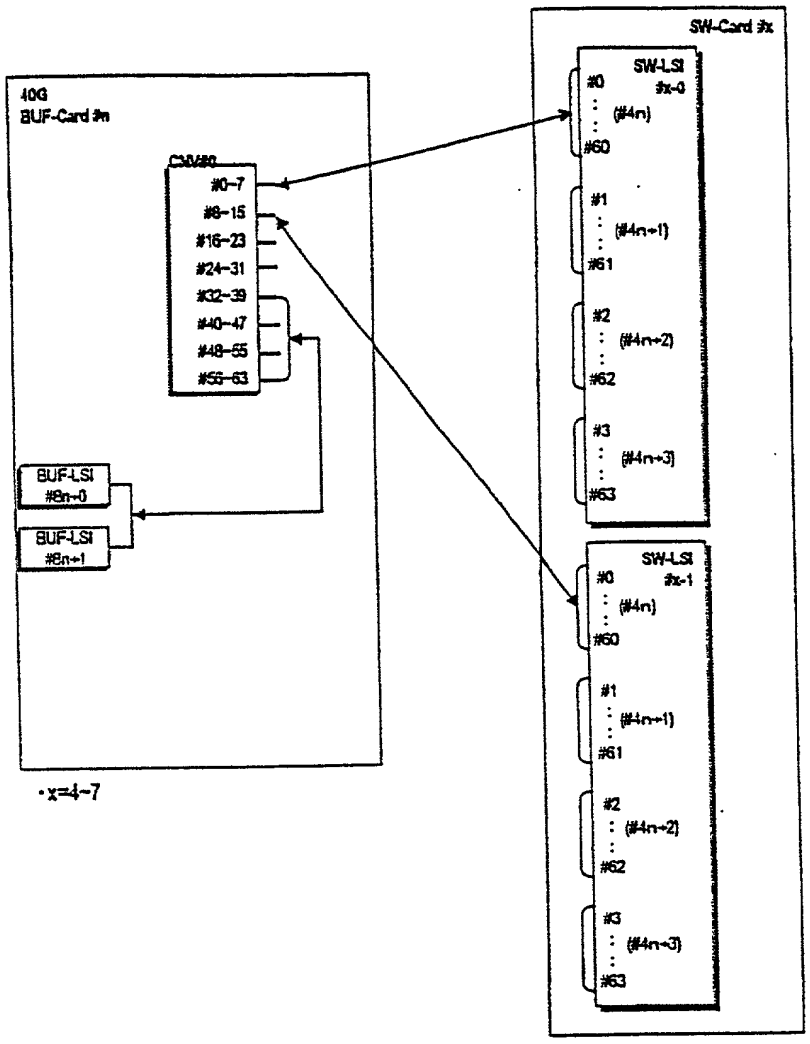

40G
BUF-Card #n
#0-7
#8-15
#16-23
#24-31
#32-39
#40-47
#48-55
#56-63
BUF-LSI
#8n+0
BUF-LSI
#8n+1
SW-Card #x
SW-LSI
#0
#x-0
(#4n)
#60
#1
(#4n+1)
#61
#2
(#4n+2)
#62
#3
(#4n+3)
#63
SW-LSI
#0
#x-1
(#4n)
#60
#1
(#4n+1)
#61
#2
(#4n+2)
#62
#3
(#4n+3)
#63
・x=4-7

FIG. 70

TABLE 7 CNV EXTERNAL TERMINAL CONNECTION CONFIGURATION

EXTERNAL TERMINAL No. (DAT#)	CONNECTION DESTINATION		
	Card (TYPE, No.)	LSI No.	EXTERNAL TERMINAL No.
00	SW#0	0	4n
01	SW#1	0	4n
02	SW#2	0	4n
03	SW#3	0	4n
04	SW#4	0	4n
05	SW#5	0	4n
06	SW#6	0	4n
07	SW#7	0	4n
08	SW#0	1	4n
09	SW#1	1	4n
10	SW#2	1	4n
11	SW#3	1	4n
12	SW#4	1	4n
13	SW#5	1	4n
14	SW#6	1	4n

FIG. 71

EXTERNAL TERMINAL No. (DAT#)	CONNECTION DESTINATION		
	Card (TYPE, No.)	LSI No.	EXTERNAL TERMINAL No.
15	SW#7	1	4n
16	SW#0	0	4n+1
17	SW#1	0	4n+1
18	SW#2	0	4n+1
19	SW#3	0	4n+1
20	—	—	—
21	—	—	—
22	—	—	—
23	—	—	—
24	SW#0	1	4n+1
25	SW#1	1	4n+1
26	SW#2	1	4n+1
27	SW#3	1	4n+1
28	—	—	—
29	—	—	—
30	—	—	—
31	—	—	—
32	SW#0	0	4n+2
33	SW#1	0	4n+2
34	—	—	—
35	—	—	—
36	BUF#n	8n	0
37	BUF#n	8n	1
38	BUF#n	8n	2
39	BUF#n	8n	3
40	SW#0	1	4n+2
41	SW#1	1	4n+2
42	—	—	—
43	—	—	—
44	BUF#n	8n+1	0
45	BUF#n	8n+1	1
46	BUF#n	8n+1	2
47	BUF#n	8n+1	3
48	SW#0	0	4n+3
49	SW#1	0	4n+3
50	—	—	—
51	—	—	—
52	BUF#n	8n	4
53	BUF#n	8n	5
54	BUF#n	8n	6
55	BUF#n	8n	7
56	SW#0	1	4n+3
57	SW#1	1	4n+3
58	—	—	—
59	—	—	—
60	BUF#n	8n+1	4

FIG. 72

EXTERNAL TERMINAL No. (DAT#)	CONNECTION DESTINATION		
	Card (TYPE, No.)	LSI No.	EXTERNAL TERMINAL No.
61	BUF#n	8n+1	5
62	BUF#n	8n+1	6
63	BUF#n	8n+1	7
RDD 0	SW#R	0	4n
RDD 1	SW#R	1	4n
RDD 2	SW#R	0	4n+1
RDD 3	SW#R	1	4n+1
RDD 4	SW#R	0	4n+2
RDD 5	SW#R	1	4n+2
RDD 6	SW#R	0	4n+3
RDD 7	SW#R	1	4n+3

(*) n; BUFFER CARD No. (0～7)
-; UNCONNECTED

FIG. 73

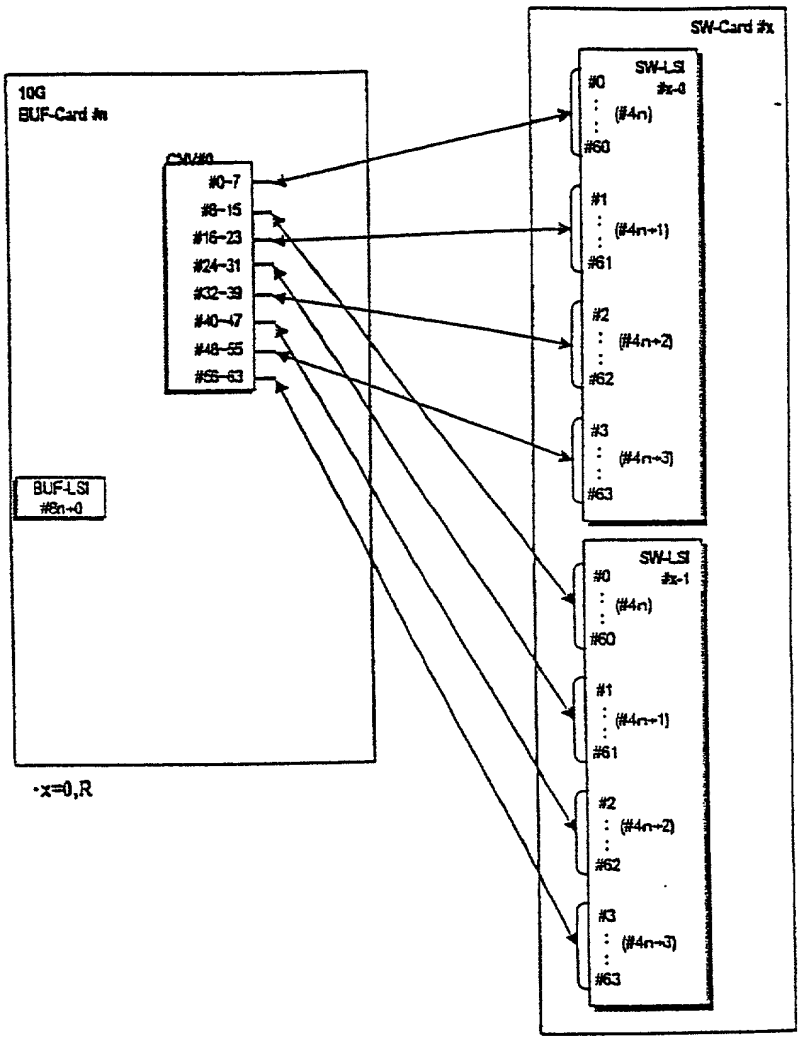

10G
BUF-Card #n
#0-7
#8-15
#16-23
#24-31
#32-39
#40-47
#48-55
#56-63
BUF-LSI
#8n+0
·x=0,R
SW-Card #x
SW-LSI
#x-0
#0
(#4n)
#60
#1
(#4n+1)
#61
#2
(#4n+2)
#62
#3
(#4n+3)
#63
SW-LSI
#x-1
#0
(#4n)
#60
#1
(#4n+1)
#61
#2
(#4n+2)
#62
#3
(#4n+3)
#63

FIG. 74

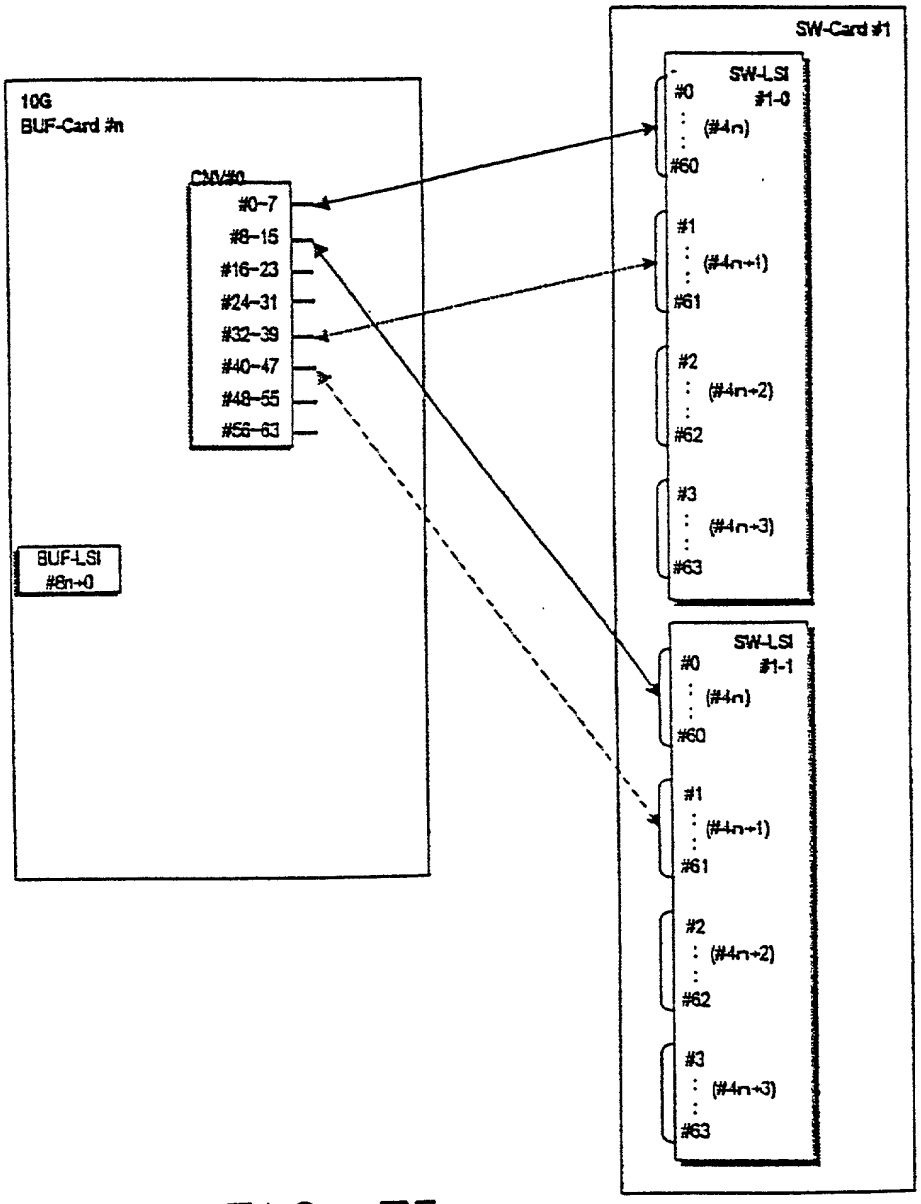

10G
BUF-Card #n
C2C#0
#0-7
#8-15
#16-23
#24-31
#32-39
#40-47
#48-55
#56-63
BUF-LSI
#8n+0
SW-Card #1
SW-LSI
#0
#1-0
(#4n)
#60
#1
(#4n+1)
#61
#2
(#4n+2)
#62
#3
(#4n+3)
#63
SW-LSI
#0
#1-1
(#4n)
#60
#1
(#4n+1)
#61
#2
(#4n+2)
#62
#3
(#4n+3)
#63

FIG. 75

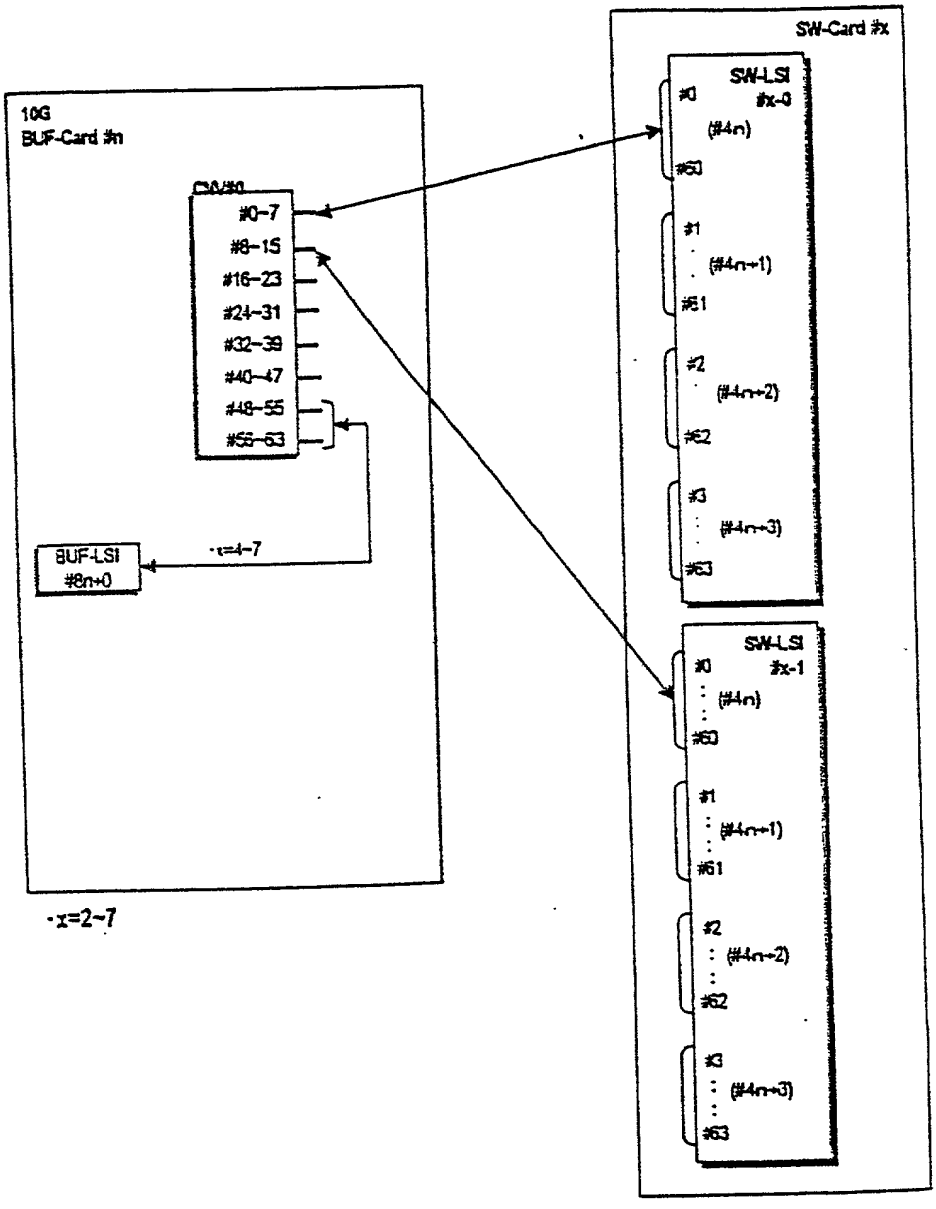

10G
BUF-Card #n
CH#0
#0-7
#8-15
#16-23
#24-31
#32-39
#40-47
#48-55
#56-63
BUF-LSI
#8n+0
x=4-7
x=2-7
SW-Card #x
SW-LSI
#x-0
#0
(#4n)
#60
#1
(#4n+1)
#61
#2
(#4n+2)
#62
#3
(#4n+3)
#63
SW-LSI
#x-1
#0
(#4n)
#60
#1
(#4n+1)
#61
#2
(#4n+2)
#62
#3
(#4n+3)
#63

FIG. 76

TABLE 8 CNV EXTERNAL TERMINAL CONNECTION CONFIGURATION

EXTERNAL TERMINAL No. (DAT#)	CONNECTION DESTINATION		
	Card (TYPE, No.)	LSI No.	EXTERNAL TERMINAL No.
00	SW#0	0	4n
01	SW#1	0	4n
02	SW#2	0	4n
03	SW#3	0	4n
04	SW#4	0	4n
05	SW#5	0	4n
06	SW#6	0	4n
07	SW#7	0	4n
08	SW#0	1	4n
09	SW#1	1	4n
10	SW#2	1	4n
11	SW#3	1	4n
12	SW#4	1	4n
13	SW#5	1	4n
14	SW#6	1	4n

FIG. 77

EXTERNAL TERMINAL No. (DAT#)	CONNECTION DESTINATION		
	Card (TYPE, No.)	LSI No.	EXTERNAL TERMINAL No.
15	SW#7	1	4n
16	SW#0	0	4n+1
17	—	—	—
18	—	—	—
19	—	—	—
20	—	—	—
21	—	—	—
22	—	—	—
23	—	—	—
24	SW#0	1	4n+1
25	—	—	—
26	—	—	—
27	—	—	—
28	—	—	—
29	—	—	—
30	—	—	—
31	—	—	—
32	SW#0	0	4n+2
33	SW#1	0	4n+2
34	—	—	—
35	—	—	—
36	BUF#n	8n	0
37	BUF#n	8n	1
38	BUF#n	8n	2
39	BUF#n	8n	3
40	SW#0	1	4n+2
41	SW#1	1	4n+2
42	—	—	—
43	—	—	—
44	—	—	—
45	—	—	—
46	—	—	—
47	—	—	—
48	SW#0	0	4n+3
49	—	—	—
50	—	—	—
51	—	—	—
52	BUF#n	8n	4
53	BUF#n	8n	5
54	BUF#n	8n	6
55	BUF#n	8n	7
56	SW#0	1	4n+3
57	—	—	—
58	—	—	—
59	—	—	—
60	—	—	—

FIG. 78

EXTERNAL TERMINAL No. (DAT#)	CONNECTION DESTINATION		
	Card (TYPE, No.)	LSI No.	EXTERNAL TERMINAL No.
61	—	—	—
62	—	—	—
63	—	—	—
RDD 0	SW#R	0	4n
RDD 1	SW#R	1	4n
RDD 2	SW#R	0	4n+1
RDD 3	SW#R	1	4n+1
RDD 4	SW#R	0	4n+2
RDD 5	SW#R	1	4n+2
RDD 6	SW#R	0	4n+3
RDD 7	SW#R	1	4n+3

(*) n; BUFFER CARD No. (0~7)
-; UNCONNECTED

FIG. 79

TABLE 9 OFFSET SETTING REGISTER TABLE (SW#0/1)

PORT No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
0	0	0	0	0
1	0	0	0	1
2	0	0	2	2
3	0	0	2	3
4	0	0	0	0
5	0	0	0	1
6	0	0	2	2
7	0	0	2	3
8	0	0	0	0
9	0	0	0	1
10	0	0	2	2
11	0	0	2	3
12	0	0	0	0
13	0	0	0	1
14	0	0	2	2
15	0	0	2	3
16	0	0	0	0
17	0	0	0	1
18	0	0	2	2
19	0	0	2	3
20	0	0	0	0
21	0	0	0	1
22	0	0	2	2
23	0	0	2	3
24	0	0	0	0
25	0	0	0	1
26	0	0	2	2
27	0	0	2	3
28	0	0	0	0
29	0	0	0	1
30	0	0	2	2
31	0	0	2	3

PORT No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
32	0	0	0	0
33	0	0	0	1
34	0	0	2	2
35	0	0	2	3
36	0	0	0	0
37	0	0	0	1
38	0	0	2	2
39	0	0	2	3
40	0	0	0	0
41	0	0	0	1
42	0	0	2	2
43	0	0	2	3
44	0	0	0	0
45	0	0	0	1
46	0	0	2	2
47	0	0	2	3
48	0	0	0	0
49	0	0	0	1
50	0	0	2	2
51	0	0	2	3
52	0	0	0	0
53	0	0	0	1
54	0	0	2	2
55	0	0	2	3
56	0	0	0	0
57	0	0	0	1
58	0	0	2	2
59	0	0	2	3
60	0	0	0	0
61	0	0	0	1
62	0	0	2	2
63	0	0	2	3

FIG. 80

◆160G Buffer-Card

TABLE 10 OFFSET SETTING REGISTER TABLE (CNV#0/1)

PORT No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
0	64	CONFIGURATION NOT ALLOWED		
1	66			
2	68			
3	70			
4	72			
5	74			
6	76			
7	78			
8	65			
9	67			
10	69			
11	71			
12	73			
13	75			
14	77			
15	79			
16	96			
17	98			
18	100			
19	102			
20	104			
21	106			
22	108			
23	110			
24	97			
25	99			
26	101			
27	103			
28	105			
29	107			
30	109			
31	111			

PORT No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
32	0	CONFIGURATION NOT ALLOWED		
33	2			
34	4			
35	6			
36	8			
37	10			
38	12			
39	14			
40	1			
41	3			
42	5			
43	7			
44	9			
45	11			
46	13			
47	15			
48	32			
49	34			
50	36			
51	38			
52	40			
53	42			
54	44			
55	46			
56	33			
57	35			
58	37			
59	39			
60	41			
61	43			
62	45			
63	47			

FIG. 81

◆80G Buffer-Card

TABLE 11 OFFSET SETTING REGISTER TABLE (CNV#0)

PORT No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
0	—	—	CONFIGURATION NOT ALLOWED	
1	—	—		
2	—	—		
3	—	—		
4	—	—		
5	—	—		
6	—	—		
7	—	—		
8	—	—		
9	—	—		
10	—	—		
11	—	—		
12	—	—		
13	—	—		
14	—	—		
15	—	—		
16	—	—		
17	—	—		
18	—	—		
19	—	—		
20	—	—		
21	—	—		
22	—	—		
23	—	—		
24	—	—		
25	—	—		
26	—	—		
27	—	—		
28	—	—		
29	—	—		
30	—	—		
31	—	—		

PORT No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
32	0	0	CONFIGURATION NOT ALLOWED	
33	2	2		
34	4	4		
35	6	6		
36	8	16		
37	10	18		
38	12	20		
39	14	22		
40	1	32		
41	3	34		
42	5	36		
43	7	38		
44	9	48		
45	11	50		
46	13	52		
47	15	54		
48	32	64		
49	34	66		
50	36	68		
51	38	70		
52	40	80		
53	42	82		
54	44	84		
55	46	86		
56	33	96		
57	35	98		
58	37	100		
59	39	102		
60	41	112		
61	43	114		
62	45	116		
63	47	118		

(*) -; ARBITRARY SETTING VALUE DUE TO UNCONNECTION

FIG. 82

TABLE 12 OFFSET SETTING REGISTER TABLE (CNV#1)

PORT No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
0	64	64	CONFIGURATION NOT ALLOWED	
1	66	66		
2	68	68		
3	70	70		
4	72	—		
5	74	—		
6	76	—		
7	78	—		
8	65	72		
9	67	74		
10	69	76		
11	71	78		
12	73	—		
13	75	—		
14	77	—		
15	79	—		
16	96	80		
17	98	82		
18	100	84		
19	102	86		
20	104	—		
21	106	—		
22	108	—		
23	110	—		
24	97	88		
25	99	90		
26	101	92		
27	103	94		
28	105	—		
29	107	—		
30	109	—		
31	111	—		

PORT No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
32	—	96	CONFIGURATION NOT ALLOWED	
33	—	98		
34	—	100		
35	—	102		
36	—	—		
37	—	—		
38	—	—		
39	—	—		
40	—	104		
41	—	106		
42	—	108		
43	—	110		
44	—	—		
45	—	—		
46	—	—		
47	—	—		
48	—	112		
49	—	114		
50	—	116		
51	—	118		
52	—	—		
53	—	—		
54	—	—		
55	—	—		
56	—	120		
57	—	122		
58	—	124		
59	—	126		
60	—	—		
61	—	—		
62	—	—		
63	—	—		

(*) -; ARBITRARY SETTING VALUE DUE TO UNCONNECTION

FIG. 83

◆40G Buffer-Card

TABLE 13 OFFSET SETTING REGISTER TABLE (CNV#0)

PORT No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
0	72	72	72	CONFIG-URATION NOT ALLOWED
1	74	74	74	
2	76	76	—	
3	78	78	—	
4	104	—	—	
5	106	—	—	
6	108	—	—	
7	110	—	—	
8	73	104	76	
9	75	106	78	
10	77	108	—	
11	79	110	—	
12	105	—	—	
13	107	—	—	
14	109	—	—	
15	111	—	—	
16	—	88	88	
17	—	90	90	
18	—	92	—	
19	—	94	—	
20	—	—	—	
21	—	—	—	
22	—	—	—	
23	—	—	—	
24	—	120	92	
25	—	122	94	
26	—	124	—	
27	—	126	—	
28	—	—	—	
29	—	—	—	
30	—	—	—	
31	—	—	—	

PORT No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
32	—	—	104	CONFIG-URATION NOT ALLOWED
33	—	—	106	
34	—	—	—	
35	—	—	—	
36	0	0	0	
37	2	2	2	
38	4	4	16	
39	6	6	18	
40	—	—	108	
41	—	—	110	
42	—	—	—	
43	—	—	—	
44	1	32	32	
45	3	34	34	
46	5	36	48	
47	7	38	50	
48	—	—	120	
49	—	—	122	
50	—	—	—	
51	—	—	—	
52	8	16	64	
53	10	18	66	
54	12	20	80	
55	14	22	82	
56	—	—	124	
57	—	—	126	
58	—	—	—	
59	—	—	—	
60	9	48	96	
61	11	50	98	
62	13	52	112	
63	15	54	114	

(*) -; ARBITRARY SETTING VALUE DUE TO UNCONNECTION

FIG. 84

◆20G Buffer-Card

TABLE 14 OFFSET SETTING REGISTER TABLE (CNV#0)

PORT No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
0	72	72	72	72
1	74	74	74	—
2	76	76	—	—
3	78	78	—	—
4	104	—	—	—
5	106	—	—	—
6	108	—	—	—
7	110	—	—	—
8	73	104	76	74
9	75	106	78	—
10	77	108	—	—
11	79	110	—	—
12	105	—	—	—
13	107	—	—	—
14	109	—	—	—
15	111	—	—	—
16	—	88	88	76
17	—	90	90	—
18	—	92	—	—
19	—	94	—	—
20	—	—	—	—
21	—	—	—	—
22	—	—	—	—
23	—	—	—	—
24	—	120	92	78
25	—	122	94	—
26	—	124	—	—
27	—	126	—	—
28	—	—	—	—
29	—	—	—	—
30	—	—	—	—
31	—	—	—	—

PORT No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
32	—	—	104	104
33	—	—	106	—
34	—	—	—	—
35	—	—	—	—
36	0	0	0	0
37	2	2	2	16
38	4	4	16	32
39	6	6	18	48
40	—	—	108	106
41	—	—	110	—
42	—	—	—	—
43	—	—	—	—
44	—	—	—	—
45	—	—	—	—
46	—	—	—	—
47	—	—	—	—
48	—	—	—	108
49	—	—	—	—
50	—	—	—	—
51	—	—	—	—
52	8	16	64	64
53	10	18	66	80
54	12	20	80	96
55	14	22	82	112
56	—	—	—	110
57	—	—	—	—
58	—	—	—	—
59	—	—	—	—
60	—	—	—	—
61	—	—	—	—
62	—	—	—	—
63	—	—	—	—

(*) -; ARBITRARY SETTING VALUE DUE TO UNCONNECTION

FIG. 85

SW-CARD CONFIGURATION	REGISTER SETTING VALUE
8 CARDS (2.56T)	2N
4 CARDS (1.28T)	8×⌊N/4⌋+N mode4
2 CARDS (640G)	8×⌊N/4⌋+N mode2
1 CARDS (320G)	8×⌊N/4⌋+N mode1

(⌊N/4⌋ INDICATES QUOTIENT (POSITIVE INTEGER) OBTAINED BY DIVIDING N BY 4)

FIG. 86

◆160G Buffer-Card

TABLE 15 SELECTOR SETTING REGISTER TABLE (CNV#0/1)

PORT No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
0	ALL 1	CONFIGURATION NOT ALLOWED		
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				
17				
18				
19				
20				
21				
22				
23				
24				
25				
26				
27				
28				
29				
30				
31				

PORT No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
32	ALL 1	CONFIGURATION NOT ALLOWED		
33				
34				
35				
36				
37				
38				
39				
40				
41				
42				
43				
44				
45				
46				
47				
48				
49				
50				
51				
52				
53				
54				
55				
56				
57				
58				
59				
60				
61				
62				
63				

FIG. 87

◆80G Buffer-Card

TABLE 16 SELECTOR SETTING REGISTER TABLE (CNV#0)

PORT No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
01		1	CONFIGURATION NOT ALLOWED	
11		1		
2	—	1		
31		1		
41		—		
51		—		
61		—		
71		—		
81		1		
91		1		
10	1	1		
11	1	1		
12	1	—		
13	1	—		
14	1	—		
15	1	—		
16	1	1		
17	1	1		
18	1	1		
19	1	1		
20	1	—		
21	1	—		
22	1	—		
23	1	—		
24	1	1		
25	1	1		
26	1	1		
27	1	1		
28	1	—		
29	1	—		
30	1	—		
31	1	—		

PORT No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
32	0	1	CONFIGURATION NOT ALLOWED	
33	0	1		
34	0	1		
35	0	1		
36	—	—		
37	—	—		
38	—	—		
39	—	—		
40	0	1		
41	0	1		
42	0	1		
43	0	1		
44	—	—		
45	—	—		
46	—	—		
47	—	—		
48	0	1		
49	0	1		
50	0	1		
51	0	1		
52	—	—		
53	—	—		
54	—	—		
55	—	—		
56	0	1		
57	0	1		
58	0	1		
59	0	1		
60	—	—		
61	—	—		
62	—	—		
63	—	—		

(*) -; ARBITRARY SETTING VALUE DUE TO UNCONNECTION

FIG. 88

TABLE 17 SELECTOR SETTING REGISTER TABLE (CNV#1)

PORT No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
0	—	—	CONFIGURATION NOT ALLOWED	
1	—	—		
2	—	—		
3	—	—		
4	—	—		
5	—	—		
6	—	—		
7	—	—		
8	—	—		
9	—	—		
10	—	—		
11	—	—		
12	—	—		
13	—	—		
14	—	—		
15	—	—		
16	—	—		
17	—	—		
18	—	—		
19	—	—		
20	—	—		
21	—	—		
22	—	—		
23	—	—		
24	—	—		
25	—	—		
26	—	—		
27	—	—		
28	—	—		
29	—	—		
30	—	—		
31	—	—		

PORT No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
32	1	1	CONFIGURATION NOT ALLOWED	
33	1	1		
34	1	1		
35	1	1		
36	1	1		
37	1	1		
38	1	1		
39	1	1		
40	1	1		
41	1	1		
42	1	1		
43	1	1		
44	1	1		
45	1	1		
46	1	1		
47	1	1		
48	1	1		
49	1	1		
50	1	1		
51	1	1		
52	1	1		
53	1	1		
54	1	1		
55	1	1		
56	1	1		
57	1	1		
58	1	1		
59	1	1		
60	1	1		
61	1	1		
62	1	1		
63	1	1		

(*) -; ARBITRARY SETTING VALUE DUE TO UNCONNECTION

FIG. 89

◆40G Buffer-Card

TABLE 18 SELECTOR SETTING REGISTER TABLE (CNV#0)

PORT No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
0	1	1	1	CONFIG-URATION NOT ALLOWED
1	1	1	1	
2	1	1	—	
3	1	1	—	
4	1	—	—	
5	1	—	—	
6	1	—	—	
7	1	—	—	
8	1	1	1	
9	1	1	1	
10	1	1	—	
11	1	1	—	
12	1	—	—	
13	1	—	—	
14	1	—	—	
15	1	—	—	
16	0	1	1	
17	0	1	1	
18	0	1	—	
19	0	1	—	
20	—	—	—	
21	—	—	—	
22	—	—	—	
23	—	—	—	
24	0	1	1	
25	0	1	1	
26	—	1	—	
27	—	1	—	
28	—	—	—	
29	—	—	—	
30	—	—	—	
31	—	—	—	

PORT No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
32	0	0	1	CONFIG-URATION NOT ALLOWED
33	0	0	1	
34	—	—	—	
35	—	—	—	
36	1	1	1	
37	1	1	1	
38	1	1	1	
39	1	1	1	
40	0	0	1	
41	0	0	1	
42	—	—	—	
43	—	—	—	
44	1	1	1	
45	1	1	1	
46	1	1	1	
47	1	1	1	
48	0	0	1	
49	0	0	1	
50	—	—	—	
51	—	—	—	
52	1	1	1	
53	1	1	1	
54	1	1	1	
55	1	1	1	
56	0	0	1	
57	0	0	1	
58	—	—	—	
59	—	—	—	
60	1	1	1	
61	1	1	1	
62	1	1	1	
63	1	1	1	

(*) -; ARBITRARY SETTING VALUE DUE TO UNCONNECTION

FIG. 90

◆20G Buffer-Card

TABLE 19 SELECTOR SETTING REGISTER TABLE (CNV#0)

PORT No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
0	1	1	1	1
1	1	1	1	—
2	1	1	—	—
3	1	1	—	—
4	1	—	—	—
5	1	—	—	—
6	1	—	—	—
7	1	—	—	—
8	1	1	1	1
9	1	1	1	—
10	1	1	—	—
11	1	1	—	—
12	1	—	—	—
13	1	—	—	—
14	1	—	—	—
15	1	—	—	—
16	0	0	0	1
17	—	—	—	—
18	—	—	—	—
19	—	—	—	—
20	—	—	—	—
21	—	—	—	—
22	—	—	—	—
23	—	—	—	—
24	0	0	0	1
25	—	—	—	—
26	—	—	—	—
27	—	—	—	—
28	—	—	—	—
29	—	—	—	—
30	—	—	—	—
31	—	—	—	—

PORT No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
32	0	0	1	1
33	0	0	1	—
34	—	—	—	—
35	—	—	—	—
36	1	1	1	1
37	1	1	1	1
38	1	1	1	1
39	1	1	1	1
40	0	0	1	1
41	0	0	1	—
42	—	—	—	—
43	—	—	—	—
44	—	—	—	—
45	—	—	—	—
46	—	—	—	—
47	—	—	—	—
48	0	0	0	1
49	—	—	—	—
50	—	—	—	—
51	—	—	—	—
52	1	1	1	1
53	1	1	1	1
54	1	1	1	1
55	1	1	1	1
56	0	0	0	1
57	—	—	—	—
58	—	—	—	—
59	—	—	—	—
60	—	—	—	—
61	—	—	—	—
62	—	—	—	—
63	—	—	—	—

(*) -; ARBITRARY SETTING VALUE DUE TO UNCONNECTION

FIG. 91

●160G Buffer-Card

RDD No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
0	1	CONFIGURATION NOT ALLOWED		
1	1			
2	1			
3	1			
4	0			
5	0			
6	0			
7	0			

FIG. 92

●80G Buffer-Card

・CNV#0

RDD No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
0	1	1	CONFIGURATION NOT ALLOWED	
1	1	1		
2	1	1		
3	1	1		
4	0	1		
5	0	1		
6	0	1		
7	0	1		

・CNV#1

DEFAULT VALUE IN ALL CASES (SETTING NOT REQUIRED)

●40G Buffer-Card

RDD No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
0	1	1	1	CONFIG-URATION NOT ALLOWED
1	1	1	1	
2	0	1	1	
3	0	1	1	
4	0	0	1	
5	0	0	1	
6	0	0	1	
7	0	0	1	

●20G Buffer-Card

RDD No.	SW-CARD CONFIGURATION			
	8 CARDS (2.56T)	4 CARDS (1.28T)	2 CARDS (640G)	1 CARDS (320G)
0	1	1	1	1
1	1	1	1	1
2	0	0	0	1
3	0	0	0	1
4	0	0	1	1
5	0	0	1	1
6	0	0	0	1
7	0	0	0	1

FIG. 93